APPLICATION NOTE

Application information for I2C-bus controlled TV-processor TDA933XH

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Philips
Semiconductors

Abstract

This report gives a description of the TDA933X-N1 version, together with application aspects.

Purchase of Philips I^2C components conveys a license under the I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

APPLICATION NOTE

Application information for I2C-bus controlled TV-processor TDA933XH

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Keywords

Synchronisation H/V
Single / Double scan, VGA
Geometry on vertical and E-W
Continuous cathod calibration
I^2C controlled

Date: October 1998

Summary

This report gives a description of the TDA933X together with application aspects. The TDA933X is the combination of a RGB output processor an a deflection processor, suitable for single scan, double scan and VGA.

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1. INTRODUCTION

This report gives a description of the TDA933X together with application aspects. The TDA933X is the successor of the TDA 478X RGB processor and TDA 9150 deflection processor. It has a higher degree of integration and additional features.

The TDA933X is a combination of a RGB output processor and deflection processor with I^2C control. The TDA933X matches ideal with the versatile TDA9321 (see ref. 2, 4) input processor (IF + video switches + full multistandard colour decoder) for set architectures using extra YUV processing like PAL plus and scan conversion (progressive scan or “100 Hz”).

All chips contain the RGB control processing with YUV input, 2 linear RGB inputs one of which has a blending option, deflection processing with H and V input, stable clock generation using an external X-tal/resonator, drive signal generation for horizontal & vertical deflection and East West (diode modulator).

Versions are available with VGA option, having a multi-sync mode for horizontal synchronisation between 30 - 50 kHz (or 15 - 25 kHz) and stabilised vertical amplitude independent of the vertical frequency.

The number of external components required for application is considerably less than equivalent two or three chip concepts. All necessary alignments can be done via I²C control.

The device is available in QFP 44 (Quad Flat Pack, 44 pins) package.

The complete integration of all functions on a single chip has been realised using the BIMOS technology (combined BIpolar and MOS). The high frequent bipolar process is used for video processing. The MOS process is used for all digital parts. Due to MOS components, it is possible to integrate very large time constants.

2. DEVICE INFORMATION

The TDA933X TV display processor is the combination of a RGB output processor and deflection processor

The device matches ideal with the versatile input processor TDA9321 (see ref. 2, 4, IF + video switches + full multi-system colour decoder including Pal plus helper demodulation) in set architectures with additional YUV processing like PAL plus or scan conversion (progressive scan or “100 Hz”).

Below the features available in all versions will be discussed. The additional features are described separately.

Available in all versions

RGB
- RGB control (brightness, contrast, saturation)
- Improved black current stabilisation (continuous cathode calibration)
- White point adjustment
- Blue stretch which offsets colours near white to blue
- Option to insert "blue back" when no video signal is available
- Black stretching of non standard luminance signals
- Switchable matrices for colour difference signals

Input
- YUV input
- Linear RGB input 1 with fast blanking for SCART RGB or VGA signals with full control (brightness, contrast, saturation)
- Linear RGB input 2 for TEXT / OSD with blending option for mixing YUV or RGB 1 input with TEXT / OSD. RGB input 2 has only brightness control

Synchronisation and Deflection
- Stable clock generation using an external 12 MHz ceramic resonator or X-tal
- Suitable for single scan (1 Fh, 1 Fv), progressive scan (2 Fh, 1 Fv) and double scan (2 Fh, 2 Fv) applications
- Horizontal synchronisation with two control loops and alignment free horizontal oscillator
- Slow start and slow stop of the horizontal drive output to enable low stress start-up and switch-off from the line circuit at nominal line supply voltage.
- Low power start-up option to generate horizontal drive pulses from only 5V/3mA supply
- Vertical count-down circuit for stable behaviour, including absence of H_D / V_D synchronisation pulses
- Horizontal and vertical geometry control
- Vertical drive optimised for DC coupled vertical output stages
- Independent horizontal and vertical linear zoom for 16:9 expand or 4:3 compress
  - Horizontal range: 65% to 100%
  - Vertical range: 75% to 138%
  - Vertical blanking for overscan
- Extended horizontal blanking to display a 4:3 picture on a 16:9 tube while blanking the standard 6% overscan which is not visible on a 4:3 tube.
- Vertical scroll for optimal display in combination with vertical zoom
- Option to switch-off in the vertical overscan to minimise visability of the discharge of the picture tube..

Control
- Full I²C bus control, as well for customer controls as for factory alignment

Power consumption
- Low power consumption

Packaging
- QFP-44 (Quad Flat Pack, 44 pins SOT 307-2)

Additional features

The additional features, varying per type, are described below. In table 1 the featuring per type is given.

Synchronisation and Deflection
- VGA multi-sync mode with a horizontal frequency range of 30 - 50 kHz (2 Fh mode) or 15 - 25 kHz (1 Fh mode) and stabilised vertical amplitude independent of the vertical frequency
- Linear DC output proportional to the horizontal frequency for power supply adaptation

Survey of additional features / type

IC version	TDA9330H	TDA9331H	TDA9332H
VGA mode		X	X
DAC output voltage (pin 25) I^2C controlled	X		X
DAC output voltage (pin 25) proportional to VGA frequency		X	

Table 1 : Survey features / type

2.1 Pinning configuration for QFP-44

The TDA933X is available in Quad Flat Package QFP-44 SOT 307-2.

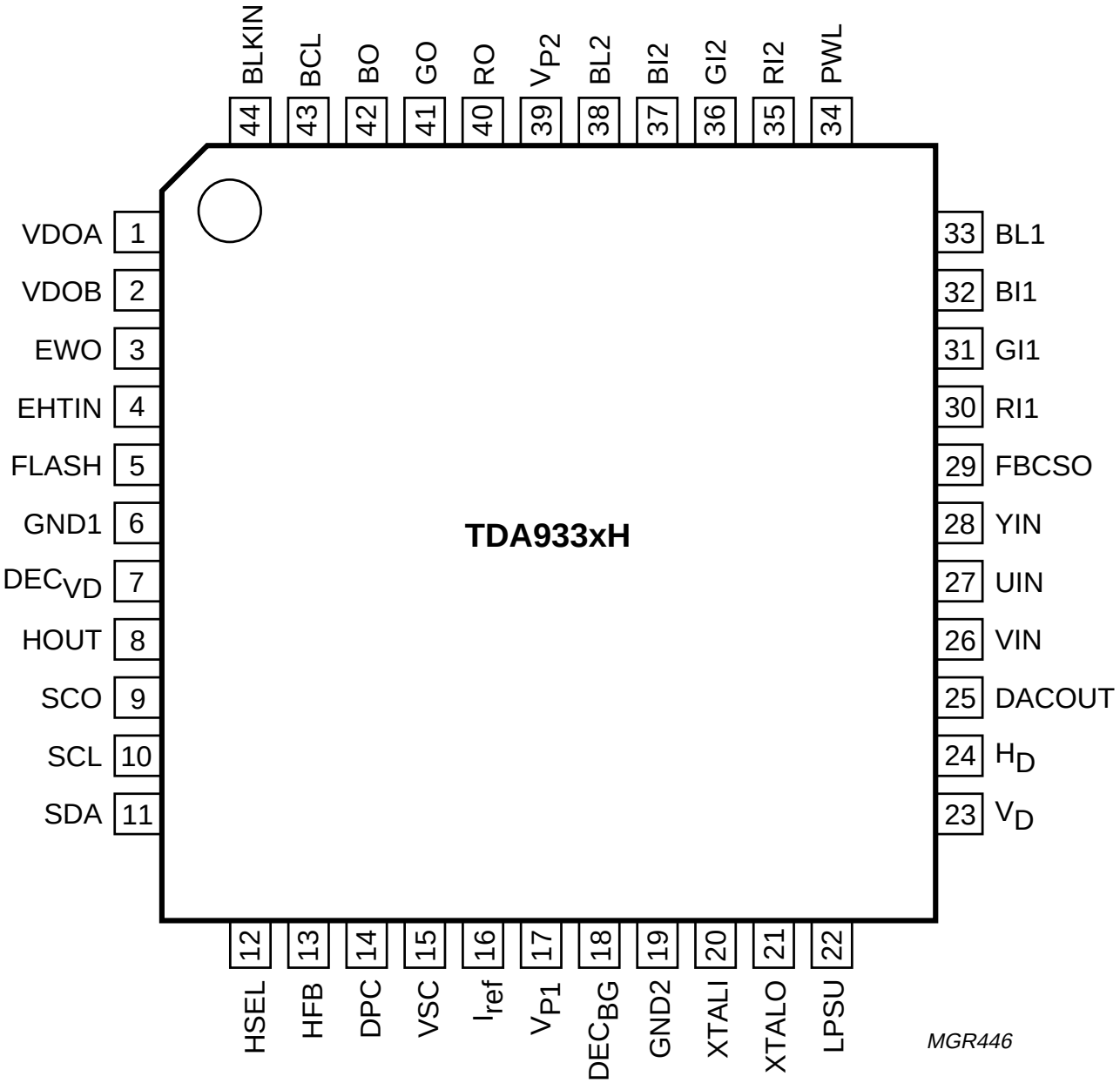


Fig 1 : Pinning diagram of QFP44

2.2 Device description per functional block

The TDA933X is organised in functional blocks. These different blocks are:

Horizontal and vertical synchronisation
Horizontal and vertical geometry
RGB processing & control
Supply decoupling
Control I²C bus

A description of each functional block has been made together with the corresponding block diagrams.
The internal circuits, connected to the pins, are shown on page 93 to 99.

In the table below, all pin numbers are given with the page number where application information can be found.

Pin	***Page***	***Pin***	***Page***	***Pin***	***Page***	***Pin***	***Page***
1	69	**12**	63	**23**	71	**34**	76
2	69	**13**	63	**24**	67	**35**	74
3	70	**14**	64	**25**	68	**36**	74
4	71	**15**	71	**26**	74	**37**	74
5	61	**16**	71	**27**	74	**38**	75
6	82	**17**	82	**28**	74	**39**	82
7	82	**18**	82	**29**	81	**40**	76
8	61	**19**	82	**30**	74	**41**	76
9	62	**20**	66	**31**	74	**42**	76
10	-	**21**	66	**32**	74	**43**	76
11	-	**22**	67	**33**	74	**44**	78

Table 2 : Application info per pin number

PIN NAME	*PIN #*	*PIN DESCRIPTION*	*PAGE #*
BCL	**43**	Beam current limiting input	**76**
BI1	**32**	Blue input 1	**74**
BI2	**37**	Blue input 2	**74**
BL1	**33**	RGB 1 insertion switch input	**74**
BL2	**38**	RGB 2 insertion switch input	**75**
BLCIN	**44**	Black current input	**78**
BO	**42**	Blue out	**76**
DACOUT	**25**	DAC output	**68**
DECBG	**18**	Bandgap Decoupling	**82**
DIGSUP	**7**	Digital supply decoupling	**82**
DPC	**14**	PHI-2 dynamic phase compensation input	**64**
EHTIN	**4**	EHT tracking / overvoltage protection	**71**
EWOUT	**3**	EW drive	**70**
FBCSO	**29**	Fixed beam current switch-off input	**81**
FLASH	**5**	Flash detection input	**61**
GI1	**31**	Green input 1	**74**
GI2	**36**	Green input 2	**74**
GND1	**6**	Grounding	**82**
GND2	**19**	Grounding	**82**
GO	**41**	Green output	**76**
HD	**24**	Horizontal synchronisation input	**67**
HFB	**13**	Flyback input	**63**
HOUT	**8**	Horizontal drive	**61**
HSEL	**12**	Horizontal frequency selection	**63**
IREF	**16**	Reference current	**71**
LPSU	**22**	Low power start-up	**67**
NDOA	**1**	Vertical drive	**69**
NDOB	**2**	Vertical drive	**69**
PWL	**34**	Peak white limiting capacitor	**76**
RI1	**30**	Red input 1	**74**
RI2	**35**	Red input 2	**74**
RO	**40**	RGB output	**76**
SANDC	**9**	Sandcastle output/Vertical guard input	**62**
SCL	**10**	I2C Clock line	**-**
SDA	**11**	I2C Data line	**-**
UIN	**27**	U input	**74**
VD	**23**	Vertical synchronisation input	**71**
VIN	**26**	V input	**74**
VP1	**17**	Supply	**82**
VP2	**39**	Supply	**82**
VSC	**15**	Vertical sawtooth	**71**
XTALI	**20**	Reference oscillator input	**66**
XTALO	**21**	Reference oscillator input	**66**
YIN	**28**	Y input	**74**

Table 3 : Application info per pin name

2.2.1 Horizontal synchronisation

See also the related block diagram (A 1 on page 21).

The main functions are:
* Horizontal oscillator, reference oscillator and acquisition loop (“PHI-1”)
* PHI-2 detector and sandcastle generation
* Horizontal output with slow start/stop facility
* Flash protection

*** Main function description**
Next, the main functions for sync will be described. See also the related paragraphs in the chapter I^2C bus description.

*** Horizontal oscillator, reference oscillator and acquisition loop (“PHI-1”)**
The horizontal oscillator requires no external components and is fully integrated. The oscillator consists of a VCO, running at a frequency of 880 * Fh = 880 * 15.625 kHz = 13.75 MHz.
The horizontal VCO is controlled by:
– The loop filter voltage
– The calibration voltage V_{CAL} from the reference oscillator (for free running mode)
– The voltage from the auto synchronisation loop (only for types with VGA mode)
The calibration voltage V_{CAL} which stabilises the free running frequency is generated by the 12 MHz reference oscillator block which needs an external resonator. It is also possible to use a 12 MHz X-tal as reference or to feed an external 12 MHz reference signal to pin 20.
The correct calibration of the horizontal VCO by the reference oscillator can be checked reading bit **NRF**. This bit should be checked under the following conditions, because when the horizontal VCO is not locked to the reference oscillator, the frequency of the horizontal drive can be incorrect:
– At power-on / initialisation before switching-on the horizontal drive
– After power dip (shutdown detection, **POR** = 1), re-initialisation is required

The horizontal frequency for H-drive and reference signal for the acquisition loop (“PHI-1”) and PHI-2 is derived from the horizontal VCO frequency using a divider chain. In this chain, various timing signals are derived for signal processing in all blocks.

An acquisition loop, consisting of a PLL with built-in loop filter, locks the horizontal VCO to the incoming synchronisation signal H_D using a phase detector with as input H_D and the divided VCO signal. The signal H_D is generated by the input processor (e.g TDA9321) or by scan conversion circuitry.
The loop filter is integrated. The loop speed can be increased by 30 % by decreasing the internal time constant by 30% setting I^2C bit **FAST** to 1,
Though this function is analogue to the PHI-1 loop of synchronisation circuits, this phase detector loop has only the task to synchronise the horizontal VCO with the H_D input and lacks therefore the sync separator, gating functions and different loopfilter time constants for synchronising under bad and noisy signal conditions.

Selection between 1 Fh and 2 Fh mode
The horizontal frequency can be set to 1 Fh or 2 Fh using a switchable divide-by-2 or divide-by-1 prescaler. The selection of the prescaler is hard wired for robustness. By connecting pin 12 to ground the prescaler is set to divide-by-2, giving 1 Fh horizontal frequency. By leaving pin 12 open, the prescaler is set to divide-by-1, giving 2 Fh horizontal frequency. Though this selection is meant for hard-wiring, it is possible to switch between 1 Fh and 2 Fh mode by pulling pin 12 low or not using a transistor. Because the status of pin 12 is only checked when switching on from stand-by, changing the level on pin 12 will first take effect when both stand-by bits **STB1,0** are toggled from 0 0 to 1 1. In this way, switching the level on pin 12 while the horizontal output is running will not change the horizontal output frequency, preventing damage to the horizontal deflection stage. However, for safe behaviour under various conditions (e.g. power supply dips) we advice to **switch only pin 12 while the TDA933X is in stand-by mode.**

TV-mode
When no H_D pulse is present, the free running horizontal frequency is set to 16.05 kHz (1 Fh mode) or 32.1 kHz (2 Fh mode)
In TV-mode, the horizontal oscillator range is limited to - 5 % to + 10 % to prevent damage to the deflection stage.
Also the maximum correction speed of the acquisition loop is limited to 2 µs per line in 1 Fh mode and 1 µs per line in 2 Fh mode.

VGA mode
For VGA mode, the horizontal oscillator can lock to incoming frequencies from 15 - 25 kHz in 1 Fh mode and from 30 - 50 kHz in 2 Fh mode.
When not locked to an incoming H_D pulse, the horizontal oscillator will run at its lowest frequency. When a H_D pulse is offered, a frequency difference detector will adjust the centre frequency of the horizontal VCO with a maximum speed of 100 kHz/s to the incoming frequency, after which the phase detector of the acquisition loop takes over and keeps the VCO synchronised.
Both horizontal and vertical synchronisation pulses have to be positive, so if synchronisation to different VGA standards with positive and negative sync pulses is needed, these sync signals have to be converted to positive polarity before feeding to the H_D input pin 24 and V_D input pin 23.

Coincidence detector, Synchronisation Lock bit SL
The coincidence detector detects whether the horizontal oscillator is synchronised with the incoming H_D pulse, thus whether the acquisition loop is in-lock. The output is available by I²C bus, **SL**, and can be used to check whether the loop is working correct.
Note that when the acquisition loop is disabled (see below, **POC**=1) **SL** is always 0.

Free running mode
By setting **POC** to 1, the acquisition loop is disabled and the horizontal oscillator will run at its free run frequency. The frequency is pending on the chosen mode (1 Fh or 2 Fh, see above). This frequency is stable because it is derived from the 12 MHz reference oscillator and is not disturbed by spurious signals on the H_D input.
This mode can be used for installation menus and also for stable blue mute when no valid signal is present. Because **SL** of the TDA 933X cannot be used to detect a valid input signal on the H_D input, an external coincidence detector (e.g. **IFI** or **SL** from the TDA 9321 input processor) should be used to detect the presence of a valid signal.

*** PHI-2 detector and sandcastle**
As described, the acquisition PLL (“PHI-1 loop”) synchronises the horizontal oscillator with the incoming H_D pulses. The PHI-2 loop synchronises the deflection drive to obtain a stable horizontal position of the picture on the screen.
This is necessary because due to beam current variations, the storage time of the line transistor varies. These storage time variations have to be compensated by adapting the phase of the horizontal drive, pin 8, to prevent horizontal shift of the picture on screen.
The horizontal flyback pulse is used as reference for the horizontal screen position. The PHI-2 detector compares the horizontal flyback input pulse, pin 13, with the horizontal oscillator signal and keeps the phase relation fixed. This fixes the horizontal position on the screen.
Using **HSH** (**H**orizontal **SH**ift), a fixed phase offset can be programmed for PHI-2. In this way the horizontal position of the picture can be centred on the screen.
Using **HP** (**H**orizontal **P**arallelogram), a phase offset change per line can be set. In this way, the phase offset changes from top to bottom of the screen. With this adjustment it is possible to set the vertical lines orthogonal to the horizontal lines (parallelogram correction) when the horizontal and vertical deflection yokes are not orthogonal.

The time constant of the PHI-2 loop is integrated. The correction factor K is 0.5. The correction factor is defined as the amount of correction of a phase error between flyback pulse and horizontal oscillator. With K = 0.5, the phase error is halved each line period.

For horizontal geometry correction related to varying EHT voltage, a dynamic phase correction input (pin 14) is provided. This input can be driven by the standard used circuits to measure the EHT voltage decrease for the beam current limiting function. The EHT info voltage should drop when the EHT drops. The level for no correction is 4.0 Volts.

Flyback input

The horizontal flyback input (pin 13) has two functions. The flyback pulse on this pin is used as input signal for the PHI-2 loop but also determines the horizontal blanking. For optimal performance, the voltage level at which the blanking starts is chosen low (0.3 Volt, maximum blanking time due to wider base of the flyback pulse) while for loop stability the slicing level for the PHI-2 reference is chosen higher (4.0 Volts).

The presence of a horizontal flyback pulse can be monitored by reading bit **NHF** (**N**o **H**orizontal **F**lyback pulse). In this way, the µprocessor can monitor the correct working of the horizontal deflection stage.

Sandcastle output/vertical guard input

The sandcastle output pin 9 is combined with the vertical guard input. The sandcastle signal timing is related to the H_D and V_D input signals and the flyback pulse.

Each horizontal line, a clamp pulse is generated. The delay from rising edge of the H_D to the clamp pulse start is 5.4 µs for 1 Fh and 2.7 µs for 2 Fh. The level is 4.5 volt typical. The clamp pulse width is 3.5 µs for 1 Fh and 1.8 µs for 2 Fh. The clamp pulse timing and generation is comparable to the burstkey pulse of the PHI-1 loop of the input processor. The clamp pulse has the same timing as the internal used clamp pulse for the YUV and RGB inputs.

When the flyback pulse on the flyback input pin rises above 0.3 Volt and starts the horizontal blanking, the level on the sandcastle pin rises to 2.5 volt.

During vertical retrace, the output voltage is kept at 2.5 Volts for 12 - 25 lines, pending on the horizontal and vertical frequency mode.

During scan, the output voltage is low.

The sandcastle pulse can be used as clamp and blanking reference for display generating devices like TXT decoders and PIP processors.

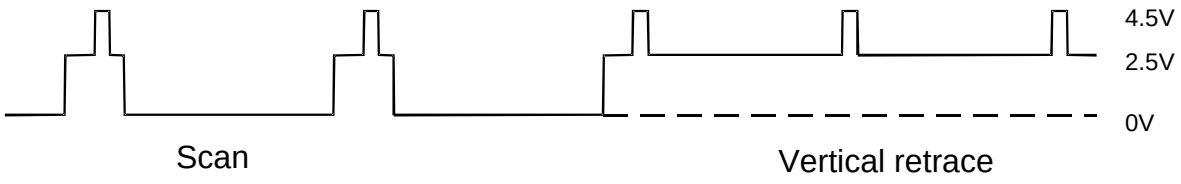


Fig 2 : Sandcastle waveform.

To prevent picture tube damage when the vertical deflection fails, a vertical guard function is added to this pin. During the vertical blanking, a current from 1 to 3 mA should be inserted to the pin during at least one line period. If such a pulse is not detected, failure of the vertical deflection circuit is assumed and the RGB outputs are blanked.

The vertical deflection family TDA8350 - TDA8358 has a special guard output pin for this function.

The vertical guard status can be read out via the bit **NDF** (**N**o vertical **D**e**F**lection). The automatic blanking of RGB during vertical guard failure can be disabled by setting bit **EVG** (**E**nable **V**ertical **G**uard) to 0. **EVG** also has to be set to 0 when the vertical guard function is not used to prevent unwanted blanking of the RGB outputs.

*** H-output and slow start/stop**

The horizontal output is the driver pin for the line deflection. It is an open collector output. Under normal operating condition the duty cycle of the output pulse is 48.2 % off (Hout=high) / 51.8 % on (Hout=low). Note that all percentages used in this chapter are related to the final cycle time of the horizontal output which can be 1 Fh, 2 Fh or varying from 15 to 50 kHz in VGA mode pending on the chosen mode.

When a horizontal flyback pulse is present at pin 13, Hout is always set high (Hout = off) irrespective the status of the output. In this way, switch-on of the line transistor during flyback time is prevented. The detection level is 0.3 Volt, so care must be taken to ensure that the level on this pin during scan is below 0.3 Volt under normal operating conditions.

Several provisions have been built-in to ease design and improve robustness of the deflection stage during switch-on and switch-off.

A build in slow start/stop circuit ensures a smooth start/stop behaviour of the line deflection and protects the line output transistor.

Switching on from stand-by via the stand-by bits STB1,0

During switch-on the horizontal output starts with a fixed off time (Hout=high) of 48.2 % while the on time (Hout=low) increases from 0% to 51.8 %. The on time increase from 0 % to 6.2 % lasts 50 ms, while the on time increase from 6.2 % to 51.8 % lasts 100 ms. These values lead in practice to a linear build-up of the EHT voltage in 150 ms while the horizontal frequency decreases from about double the final frequency to the final frequency.
Some picture tubes e.g. versions with DAF gun, are sensitive for flash-over when the EHT voltage rises too fast from 75% to 100% of the nominal EHT value. For these picture tubes, the EHT increase from 75 % to 100 % can be slowed down by setting bit **ESS** (**E**xtended **S**oft **S**tart) to 1. The on-time increase from 39 % to 51.2 % is then extended to 1000 ms. (See Fig 3).

Low power start-up

To ease the design of the stand-by power supply, a special low power start-up facility is built-in. This low power start-up mode can be activated by supplying 5 Volts to pin 22 when no 8 Volt is present on supply pins 17 and 39.
When 5 Volts is supplied, the horizontal output will start via a slow start procedure. The off time is fixed to 48.2 % and the on time is increased from 0 % to 12.5 % and remains running on this frequency. This horizontal drive should provide enough load for the power supply to wake it from stand-by mode and to build-up an 8 Volt supply using scan rectification of an auxiliary winding of the FBT for supplying pin 17 and 39 of the TDA 933X.
When the 8 Volt supply is present and the **POR** has been cleared by reading the status bytes and successful calibration of the horizontal VCO is confirmed by checking **NRF** = 0, all I^2C registers must be written including **STB1,0** = 1 1. Then the on time of Hout is increased further from 12.5 % to 51.8 % according the slow start procedure as described above.
When the H-out is not switched on from stand-by within 2 fields after **POR** is cleared, the on time is reduced from 12.5 % to 0% to switch-off safe the deflection when the 8 Volt is malfunctioning.
When the 8 Volt is present and **STB1,0** is set to 1 1, the 5 volt supply on pin 22 should be removed to ensure that H-out can be switched off completely. As long as the +5 Volt is present, H-out will remain running at 12.5 % on/ 48.2 % off when set to stand-by or when the +8 Volt is removed.
This low power pin 22 only needs 3 mA supply current typical. In this way, the stand-by power supply design can be simplified because one voltage can be used for µprocessor and low power start-up while the power needed for the TDA 933X is only 15 mW (23 mW max.) compared to 400 mW (510 mW max.) and an 8 Volt supply when the TDA 933X is started up in normal mode.

Switching off to stand-by using STB1,0

When switching-off via the stand by bits (**STB1,0**) the off time remains fixed on 48.2 % while the on time decreases from 51.2 % to 0 % in 43 ms. The on time decrease starts first after the vertical scan and vertical flyback is completed.
During the first 37 ms of the switch-off time, the RGB outputs can be driven to obtain a fixed beam current for discharging the picture tube when bit **FBC** (**F**ixed **B**eam **C**urrent switch-off) is set to 1. The monitoring of the beam current is done via the Continuous Cathode Calibration loop which stabilises the cut-off and drive for the picture tube. (see chapter RGB processing and control for details).
The visability of the picture tube discharge can be minimised by setting bit **OSO** (**O**verscan **S**witch **O**ff) to 1. When switching to stand-by, after completion of the vertical scan and vertical flyback, the vertical deflection is kept fixed in overscan so the discharge takes place in the overscan.

Switching off using mains switch

Also provisions are available when the set is switched-off via the mains switch. An external circuit should monitor the supply voltage of the deflection. When this voltage decreases, pin 29 (Fixed Beam Current Switch Off) should be pulled high. From that moment, first the vertical scan and vertical flyback is completed.
When **FBC** is set to 1, the RGB outputs are then driven to obtain a fixed beam current for discharge of the picture tube.
When **OSO** is set to 1, the vertical deflection is kept fixed in overscan to minimise visability of the discharge.

H-out will keep running on nominal frequency, but because the deflection supply voltage decreases, the EHT will decrease proportionally. H-out will continue running till the supply voltage of the TDA 933X drops below the **POR** (**P**ower **O**n **R**eset) level. Both H-out and RGB drive will then be stopped.

See also chapter RGB control, paragraph Fixed beam current discharge.

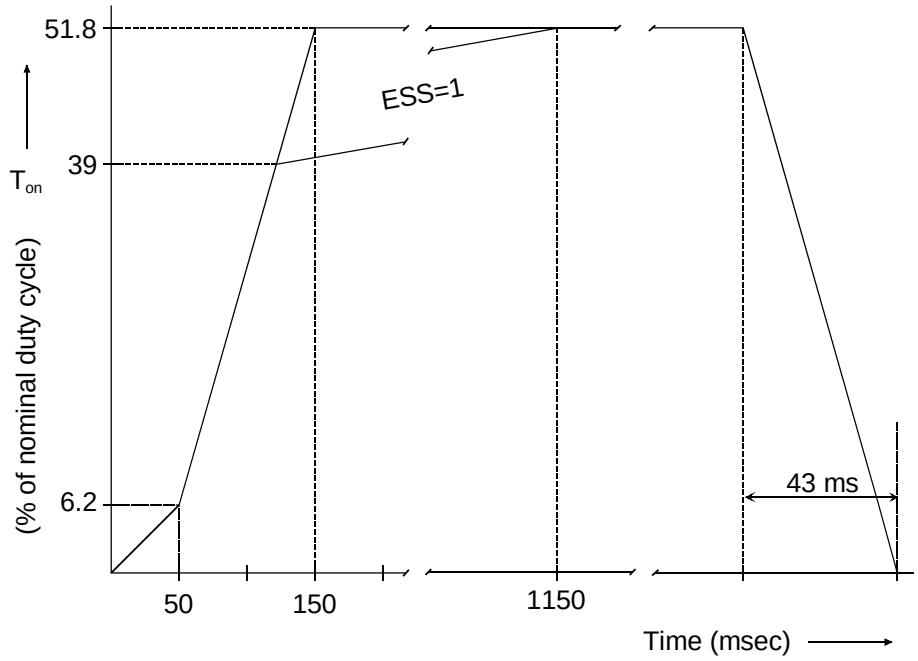
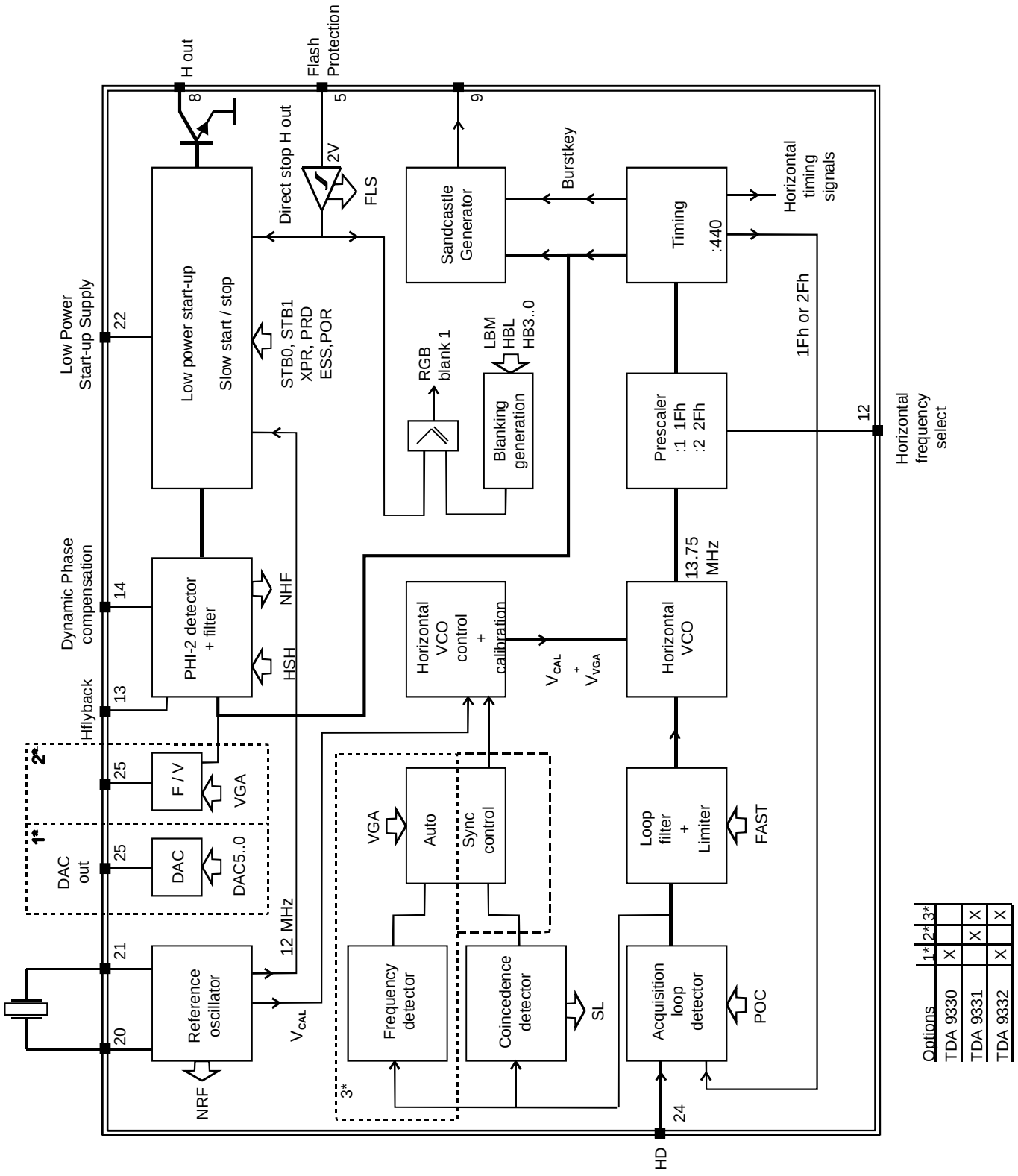


Fig 3 : Slow start / slow stop horizontal output.

*** Flash protection**
To protect the horizontal deflection stage during flash-over, the flash input pin 5 can be used. By pulling this pin above 2 Volts, the Hout is disabled immediately. When the voltage drops below 1.8 Volts, the horizontal output is started up again via the slow start procedure. This protection is hard wired and does not need intervention of the µprocessor. The status of the flash input can be read via status bit **FLS**, so the µprocessor can take additional action when needed.
An external flash detection circuit has to be applied to use this function. The hysteresis of the input prevents unstable behaviour.
For another protection facility, see paragraph “EHT compensation and overvoltage protection” in chapter “Vertical synchronisation/deflection and geometry (horizontal and vertical)”.



Options	1*	2*	3*
TDA 9330	X		
TDA 9331		X	X
TDA 9332	X		X

A 1: Block diagram: Horizontal and vertical synchronisation

2.2.2 Vertical synchronisation/deflection and geometry (horizontal & vertical)

See also the related block diagram as well as the diagrams at the end of the report.

We can distinguish the following main blocks, which will be described in more detail below:
* Vertical divider system
* Vertical sawtooth generator
* Vertical geometry processor
* Horizontal (E-W) geometry processor
* EHT tracking + overvoltage protection

*** Vertical divider system**
The divider system uses a counter that delivers the timing for the vertical ramp generator in the geometry processor. The clock is derived from the horizontal line oscillator.
The divider system synchronises on the V_D pulse on pin 23 of the TDA933x. For optimum noise margin and reliable field detection, the edges of the V_D pulse should be positioned on ¼ and ¾ of the line period referring to the rising edge of the H_D pulse as reference. (see Fig 4)
The timing of the vertical retrace for various modes will be discussed below and is also given in
Fig 5 and Fig 6 at the end of this paragraph.
Internally, a clock signal is generated running at the double frequency of the horizontal output. This signal is indicated in the figures as "CK2H" (**C**loc**K 2 H**-out) and is not related to the 2Fh frequency for double scan frequency.

TV mode
1 Fh mode:
When V_D becomes high, the following actions are taken the first following clock pulse of the CK2H clock signal:
– The vertical line counter is reset
– Detection odd/even field by checking whether the CK2H clock pulse coincides with the horizontal blanking or not
– Vertical blanking starts and lasts 22 / 22.5 lines for 50 Hz and 17 / 17.5 lines for 60 Hz signals for odd / even fields
– A vertical saw reset is generated which discharges the vertical sawtooth capacitor to the reset level (2.3 Volt). The reset time is 14 lines for 50 Hz and 10 lines for 60 Hz.

See
Fig 5 and Fig 4.

2 Fh mode
In this mode, two extra parameters can be set using **VSR** (**V**ertical **S**can **R**eference) and **VWT** (**V**ertical **W**ai**T**).
The bit **VSR** determines whether the rising edge or the falling edge of the V_D pulse is used as reference for the field detection and **VWT**.
The five bits register **VWT** sets the number of lines which the vertical sawtooth capacitor is kept to its reset level of 2.3 Volts and so determines at which line the vertical scan will start. The minimal number of lines is 8, putting a lower number in the **VWT** register will still generate 8 lines reset before the vertical scan is started. This function can be used to position the picture vertical correct for various modes of scan conversion boxes.
When V_D becomes high, the following actions are taken the first following clock pulse of the CK2H clock signal:
– The vertical line counter is reset
– Vertical blanking starts. The duration is related to the **VWT** setting.
– The vertical saw reset is started.

The actions below are executed on the timing, set by **VSR**:
VSR = 0: The first clock pulse of the CK2H clock signal, following the falling edge of the V_D pulse
VSR = 1: The first clock pulse of the CK2H clock signal, following the rising edge of the V_D pulse
– Detection odd/even field by checking whether the CK2H clock pulse coincides with the horizontal blanking or not
– Start counting the number of lines set by **VWT** before releasing the vertical saw reset and starting the vertical scan. The total reset time is pending on the reference used for **VWT**:
For **VSR** = 0, the total reset time is the number of lines V_D lasts plus the number of lines, set by **VWT**.
For **VSR** = 1, the total reset time is equal to the number of lines, set by **VWT.**

See Fig 6 and Fig 4.

VGA mode

In this mode, always the rising edge of the V_D pulse is used as reference for field detection and **VWT** irrespective of the setting of **VSR**. It is possible to use **VWT** to determine the start of vertical scan.

When V_D becomes high, the following actions are taken the first following clock pulse of the CK2H clock:

- The vertical line counter is reset
- Vertical blanking starts. The duration is related to the **VWT** setting.
- The vertical amplitude is stabilised
- Start counting the number of lines set by **VWT** before releasing the vertical saw reset and starting the vertical scan
- After 2 additional clock pulses of the CK2H clock (one line) the vertical saw reset is started. The total reset time is therefore **VWT** minus one line.

Also here, the minimal number of lines for **VWT** is 8. A lower number will still generate 8 lines reset before vertical scan is started.

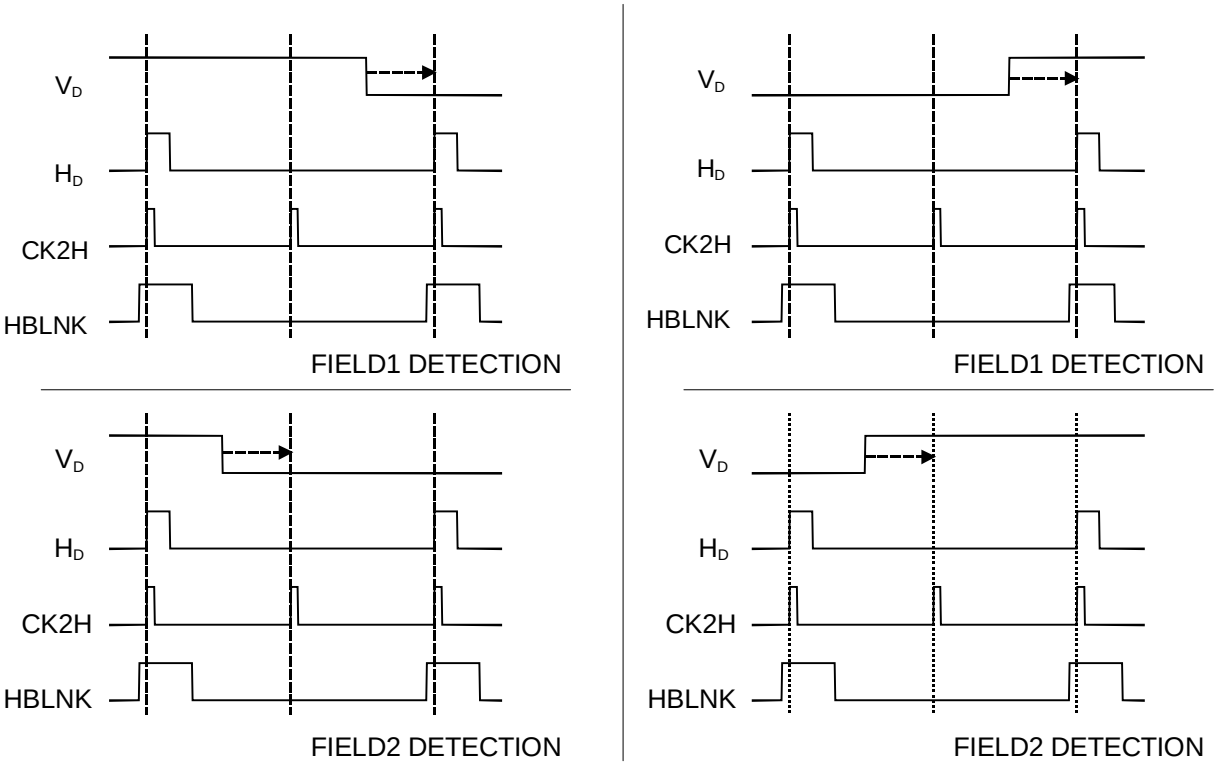


Fig 4 : Field detection mechanism for VSR=0(A) and VSR=1(B)

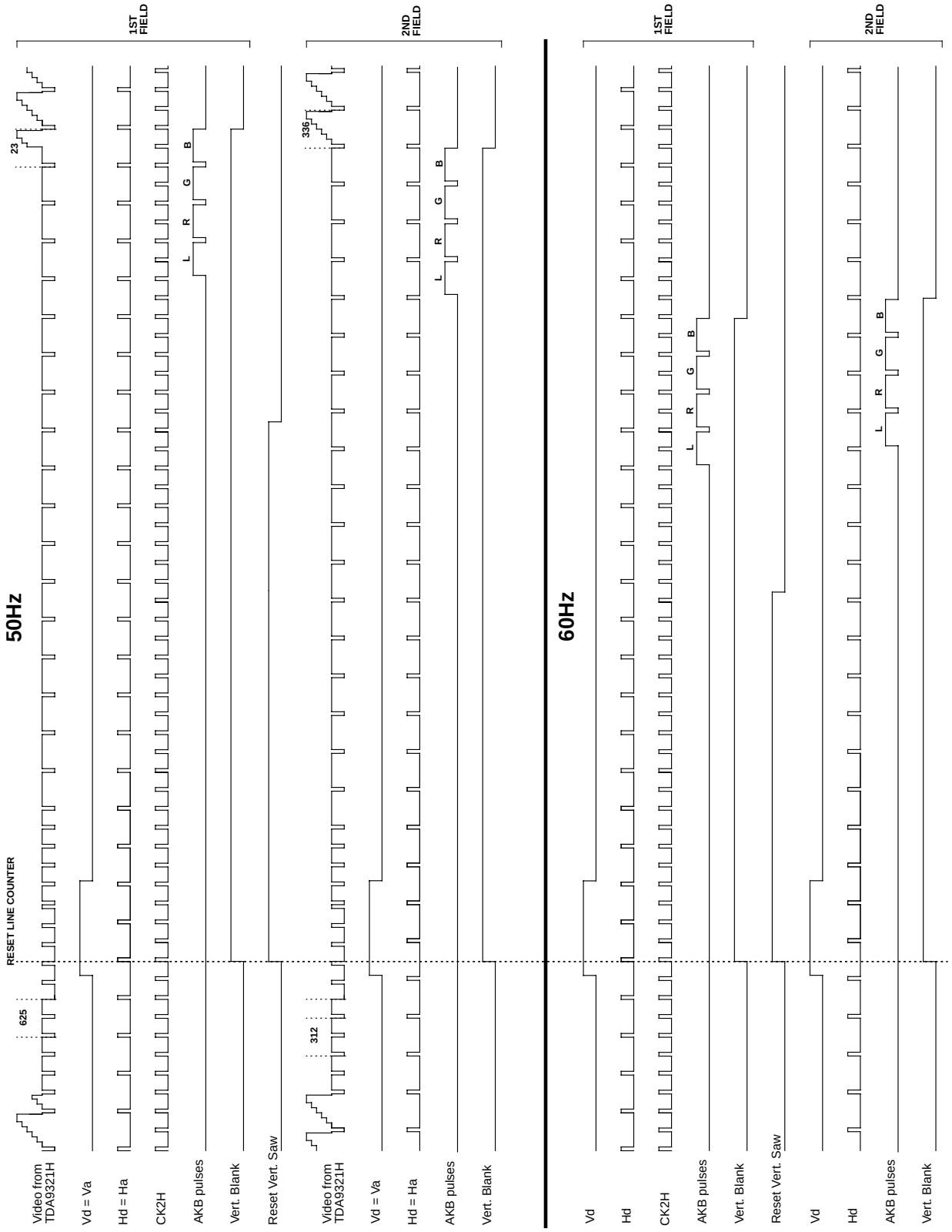


Fig 5 : 1FH Timing diagram

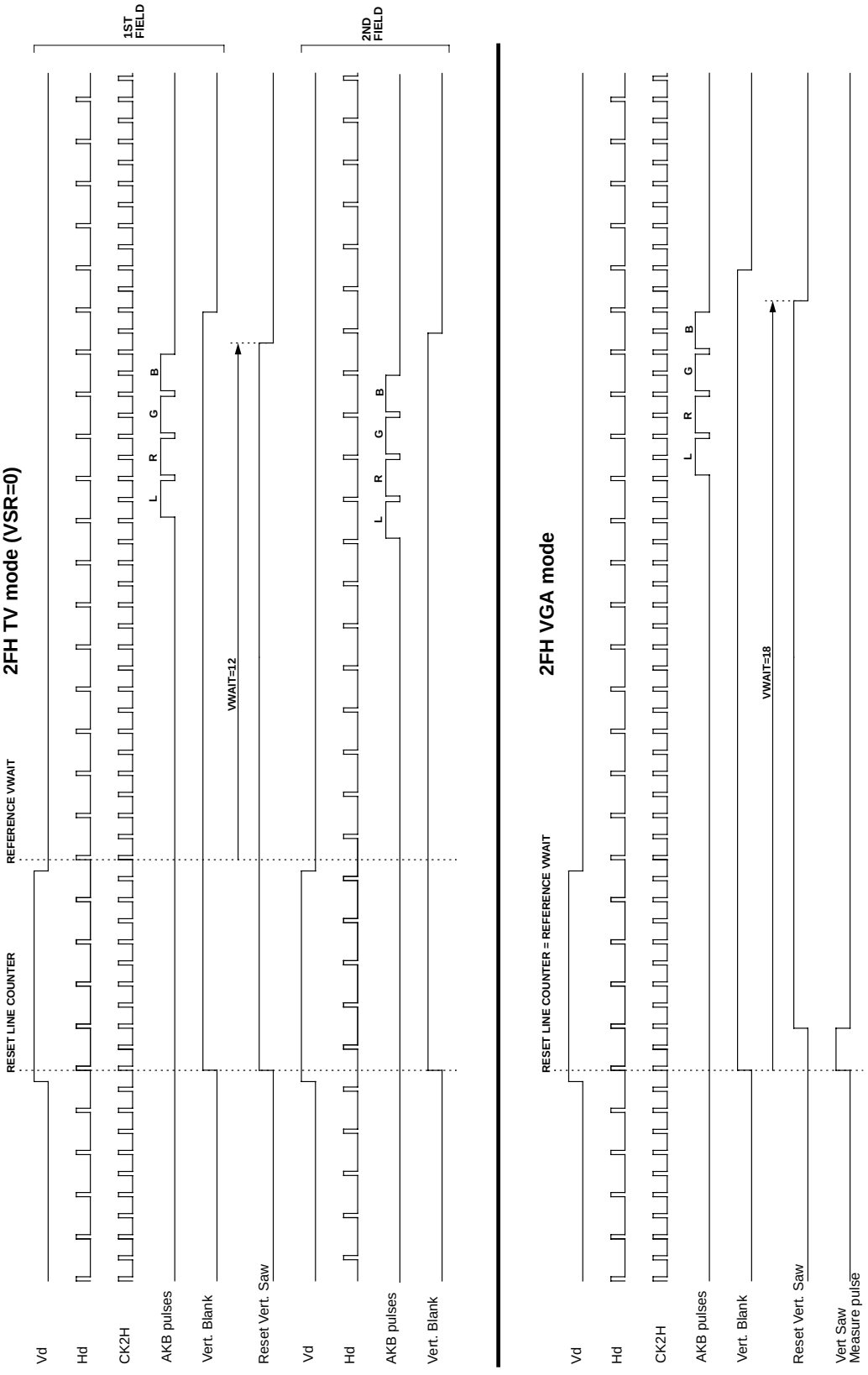


Fig 6 : 2FH Timing diagram

Vertical frequency

TV mode
In TV mode, the vertical divider can be set to four different modes by the **SVF** (**S**et **V**ertical **F**requency) and **VFF** (**V**ertical **F**ree running **F**requency) bit.. These modes determine the setting for 1 Fv or 2 Fv mode and the free running frequency in these modes when no valid V_D pulse is present

SVF	VFF	1Fh / 2Fh	Lines / field	Vertical frequency
X	0	1Fh	312.5	50 Hz
X	1	1Fh	262.5	60 Hz
0	0	2Fh	625	50 Hz
0	1	2Fh	525	60 Hz
1	0	2Fh	312.5	100 Hz
1	1	2Fh	262.5	120 Hz

VGA mode
In VGA mode, in free running mode the number of lines / field is fixed:
1 Fh VGA mode: 288 lines (55.7 Hz when also no H_D is present and Hout runs at 16.05 kHz)
2 Fh VGA mode: 576 lines (55.7 Hz when also no H_D is present and Hout runs at 32.1 kHz)

The 1 Fh mode or 2 Fh mode is set by connecting pin 12 to ground (1 Fh) or leave pin 12 open (2 Fh).

Catching ranges

TV mode
In TV-mode, the catching range is:
1 Fh, 1 Fv: 511.5 to 244 lines / field (30.5 to 64 Hz)
2 Fh, 1 Fv: 1023 to 488 lines / field (30.5 to 64 Hz)
2 Fh, 2 Fv: 511.5 to 244 lines / field (61 to 128 Hz)

VGA mode
For VGA, only the lines / field can be given. The vertical frequency is pending on the used horizontal frequency:
1 Fh VGA mode: 450 to 175 lines / field
2 Fh VGA mode: 900 to 350 lines / field
The vertical frequency range is determined by the automatic amplitude stabilisation circuit and ranges from 50 to 90 Hz.

Interlace
Interlace can be switched on and off by I²C bus **DL** (**D**e-inter**L**ace). To accommodate various TXT processors, also the choice can be made to delay the first or the second field with 0.5 line (reference is the V_D pulse) using bit **DIP** (**D**e-**I**nterlace **P**hase).

*** Vertical sawtooth generator**
The vertical sawtooth generator delivers the reference signals for vertical and horizontal geometry processor.
An accurate reference current (Iref) of 100µA is realised by means of an internal bandgap reference voltage (3.9V) and an external resistor (39kΩ). This 100µA reference current is used to derive a 16 µA current to charge the external capacitor during vertical scan (1 Fh, 50 Hz). This circuitry ensures a very linear sawtooth (Usaw) that is used for further processing on vertical and horizontal (E-W).

* **TV-mode**
The charge current for the sawtooth is automatically adapted pending on the input control bits **SVF** and **VFF** and the output control bit **FSI** (**F**ield **S**ynchronisation **I**nformation). **FSI** indicates whether the vertical frequency is 50/100 or 60/120 Hz and is only valid when a valid V_D pulse is present and **SL** (**S**ync **L**ock) = 1, indicating lock of the acquisition loop to a valid H_D input. See the table below:

SVF	VFF	FSI	1Fh / 2Fh	SL	Charge current (µA)	Frequency (Hz)
X	0	X	1Fh	0	16	50
X	1	X	1Fh	0	19	60
0	0	X	2Fh	0	16	50
0	1	X	2Fh	0	19	60
1	0	X	2Fh	0	32	100
1	1	X	2Fh	0	38	120
X	X	0	1Fh	1	16	50
X	X	1	1Fh	1	19	60
0	X	0	2Fh	1	16	50
0	X	1	2Fh	1	19	60
1	X	0	2Fh	1	32	100
1	X	1	2Fh	1	38	120

Furthermore the charge current can be adjusted with the I²C bus control, **VS** (vertical slope). The range is +/- 20% should be used to compensate for tolerance of the external capacitor. When vertical zoom is applied, **VS** can be used to vary the position of the bottom part of the picture independent from the upper part (subtitle shift)

The external capacitor is discharged during vertical retrace by the vertical divider system, see above.

VGA mode
To prevent adjustment of the vertical amplitude for various VGA frequencies, the peak to peak amplitude of the vertical sawtooth at the sawtooth capacitor is measured and the charge current is adjusted to keep the amplitude constant independent of the vertical frequency.
The frequency range from this circuit is ranging from 50 to 90 Hz.

*** Vertical geometry processor**
The sawtooth signal that is derived from the sawtooth generator can be controlled by I²C bus. Control functions are: **VA** (**V**ertical **A**mplitude), **VSH** (**V**ertical **SH**ift), **SC** (**S**-**C**orrection), **VX** (**V**ertical e**X**pand (zoom)), **VSC**(**V**ertical **SC**roll).
To prevent picture damage, a built-in blanking functions blanks the RGB outputs for vertical overscan, larger than 105%. This function is active for both **VX** and **VSC**.

The vertical geometry processor has a differential current output for a DC coupled vertical output stage (drive).
It is important to notice that the TDA933X is designed for use with a DC coupled output stage. This is the reason why a vertical linearity alignment is not necessary (and therefore not available).

A half picture blanking function (service blanking, **SBL**) is available for vertical alignment (See chapter alignment)

*** Horizontal geometry processor (E-W drive)**
The horizontal geometry signal for E-W drive can control via the I²C bus the following functions:
EW (EW-Width), **PW** (Parabola/Width), **CP** (Corner/Parabola) and **TC** (Trapezium Correction).
The EW-width adjust range is such that linear zoom is possible on the picture size when used together with vertical expand (zoom).
The horizontal geometry processor has a single-ended current output for E-W drive.

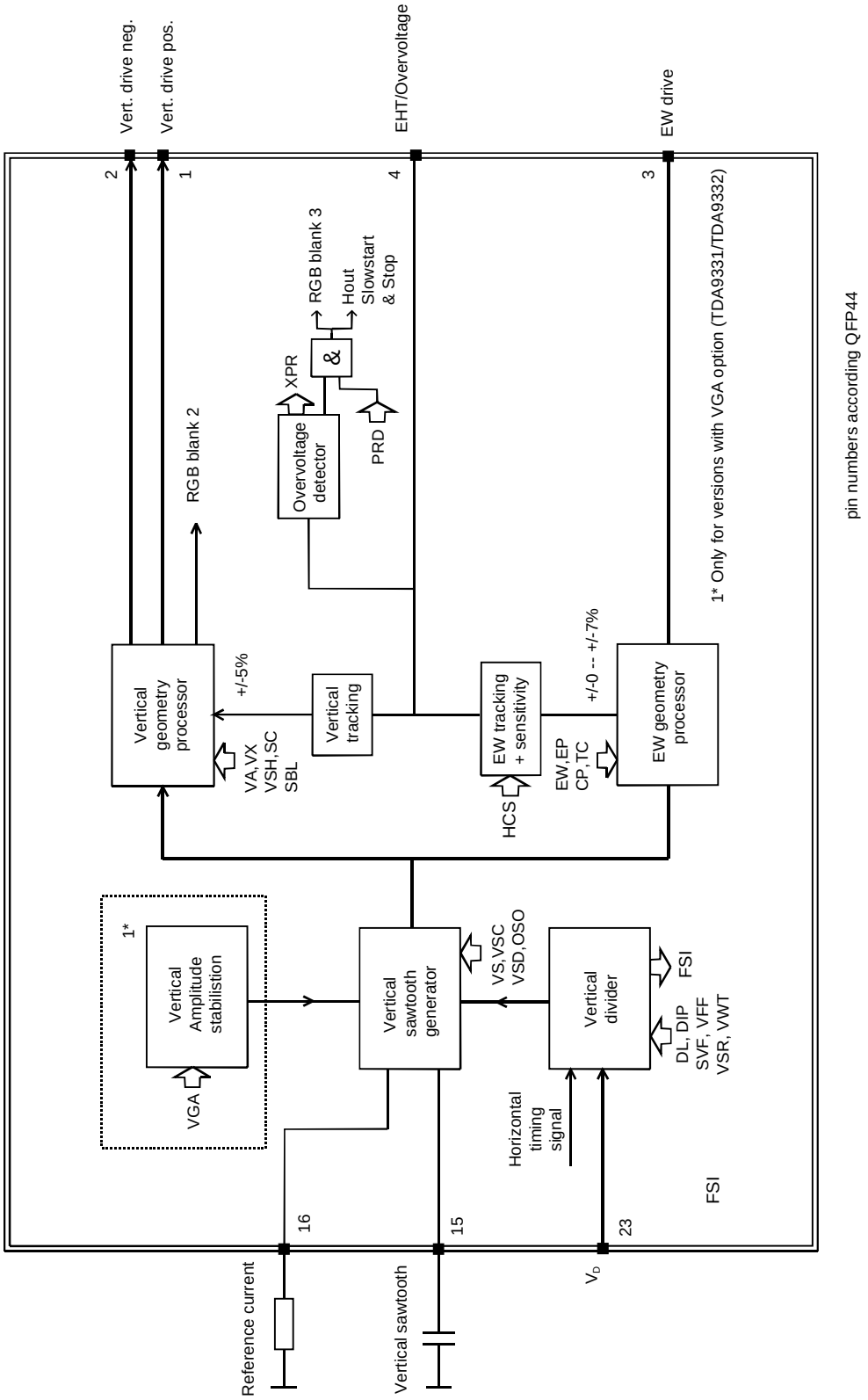
Corrections for different scan frequencies and zoom

TV mode
Once all vertical and horizontal parameters are aligned, the geometry settings do not have to be adapted when changing to other vertical or horizontal scan frequencies.
Also when using zoom (horizontal and/or vertical) and vertical scroll (**EW**, **VX**, **VSC**) the geometry will remain correct without adapting the other geometry registers.
Note: this geometry adaptation only works when the correct geometry alignment procedure (see chapter “Geometry alignment”) has been followed.

VGA mode
Also in VGA mode the geometry settings will remain correct for different horizontal and vertical frequencies. The horizontal geometry currents are proportionally adapted to the horizontal VCO frequency for this purpose.

*** EHT tracking + overvoltage protection**
Both the vertical and the E-W drive can be modulated for EHT compensation.
This tracking makes the picture size independent of EHT variations due to the beam current. The compensation range is -5 to +5 % and is fixed for the vertical deflection. Therefore the circuit should be designed for correct tracking of the vertical amplitude. The horizontal compensation can be matched to the vertical compensation by setting **HCS**. The horizontal compensation range can be set from 0 to +/-7%.

A second function of this pin is for overvoltage protection, **XPR** (**X**-ray **PR**otection). **XPR** is set to "one" when the voltage on the pin exceeds 3.9 Volts and can be read by I²C bus. The bit is internally latched and will only be cleared when **XPR** is read after the voltage at pin 4 has dropped below 3.9 Volts. This ensures that the µprocessor can monitor a short exceeding of the 3.9 Volt level.
It is possible to switch the horizontal output automatically off via slow stop for **XPR** = 1 when **PRD** (PRotection Detection mode) is set to 1. When **XPR** becomes 1, the vertical scan is completed and after the vertical retrace the H-out is switched off via the slow stop procedure and the IC is set in stand-by mode. The µprocessor can check **XPR** and decide whether to start-up the set again or to generate an error message (e.g. blinking led).



A 2: Block diagram: Geometry on vertical and E-W drive

2.2.3 RGB processing and control

See also the related block diagram as well as the diagrams at the end of the report.

This paragraph can be divided into:
-YUV/RGB selection
-RGB-control

2.2.3.1 YUV/RGB selection

The main blocks are:
- YUV/RGB 1 insertion and selection
- Y, U and V signal processing.
- RGB-adder +clamps
- Contrast control
- Black stretcher
- Blue stretcher
- RGB2 signal selection

- **Y, R-Y, B-Y/RGB 1 insertion and selection**

The luminance and colour difference input signals should be AC coupled to the input pins. These input signals are internally clamped and supplied to the YUV selection circuit. By means of the I²C bus bit **GAI** an additional 10 dB amplification can be selected.
For RGB 1 insertion, the RGB signals should be AC coupled to the input pins where they are internally clamped. These RGB inputs are meant as external (SCART) inputs in 1Fh-mode and as VGA inputs in 2Fh mode..
The RGB1 insertion signals are converted to YUV signals by means of a RGB/YUV converter. The converter uses the inverse PAL matrix, so for correct colour reproduction the PAL matrix must be selected in the Y, B-Y and R-Y processing block (see also related paragraph). The YUV signal after conversion is supplied to the YUV source selector.
The YUV Source selector is controlled by hardware by means of the RGB1 insertion input signal BL1, (by applying an external voltage at this pin) and is designed for fast switching. The switching using BL1 can be enabled via the I²C bus by bit **I**nsertion **E**nabled **1** (**IE1**). By means of the **IN1** bit the RGB1 insertion pin status can be sensed. The status is only sensed during vertical retrace, so OSD insertion of descramblers will not set the **IN1** bit.
The RGB 1 insertion inputs are linear (video) inputs.

***Y, B-Y and R-Y signal processing/matrixing**

The luminance signal is supplied to a black stretcher circuit. This circuit, which is only operational during line scan, extends the grey signal level towards the actual black level (i.e. actual black level is measured during burstkey). The amount of extension is dependent upon the difference between actual black level and the darkest part of the incoming video signal; it is thus dependent upon the IRE value of the video signal.
The darkest part of the video signal is registered on an internal-capacitor. For the black stretcher input/output characteristic, see the device specification. The black stretcher can be switched on/off via the I^2C bus **(BKS)**. The black stretcher is fully integrated so the black stretcher time constant is fixed.

The saturation of the R-Y and B-Y signals is controlled via the I²C bus **(SAT)** The control range is minimal 52dB with a 6dB (minimum) reserve above nominal saturation level , refer also to the device specification.
The colour matrix can be controlled via the I²C bus bits **(MAT)** and **(MUS)**. With the **MAT** -bit the PAL/SECAM matrix or NTSC matrix can be selected. With the **MUS** -bit selection of the Japanese NTSC matrix or USA NTSC matrix can be made.
In Fig 7 the three matrices are given (see device specification).

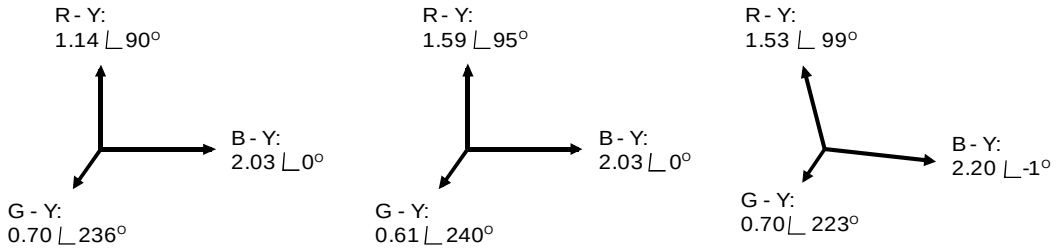


Fig 7 : Matrix options

After the R-Y and B-Y processing the signals are added with the luminance signal in order to generate the internal RGB signals. At the same time a clamping action on the internal RGB-signals takes place.

Note: When using the RGB1 input, the PAL matrix must be selected to get correct colour reproduction. The matrix, used to convert the RGB signals at RGB1 to YUV for internal processing is inverse to the PAL matrix.

***Contrast control**

Contrast can be controlled for
- The internal video signal coming from the YUV-outputs of the TDA9321 (HIP) or from the YUV outputs of a scan conversion box (100Hz converter, progressive scan converter) or PAL plus decoder.
- RGB signals inserted via the RGB1 insertion inputs.

Contrast control has no influence on the second RGB insertion inputs which will be discussed later on in this chapter. More about contrast will be given in the paragraph “RGB-controls”, in this paragraph an overview of all the controls are given
The blue back, which can be activated by the I^2C bit **EBB**, is inserted at the contrast control function. When **EBB** is set to 1, a blue screen is inserted. This function can be used for example when no valid input signal is available, which usually is indicated by the coincidence detector of the input processor part.

*** Blue stretcher**

The standard blue stretcher of the TDA993X can be activated by the I^2C bit **BLS**. The blue stretcher reduces the R- and G-signals by 14% whenever the video signal exceeds a threshold level of 80%.

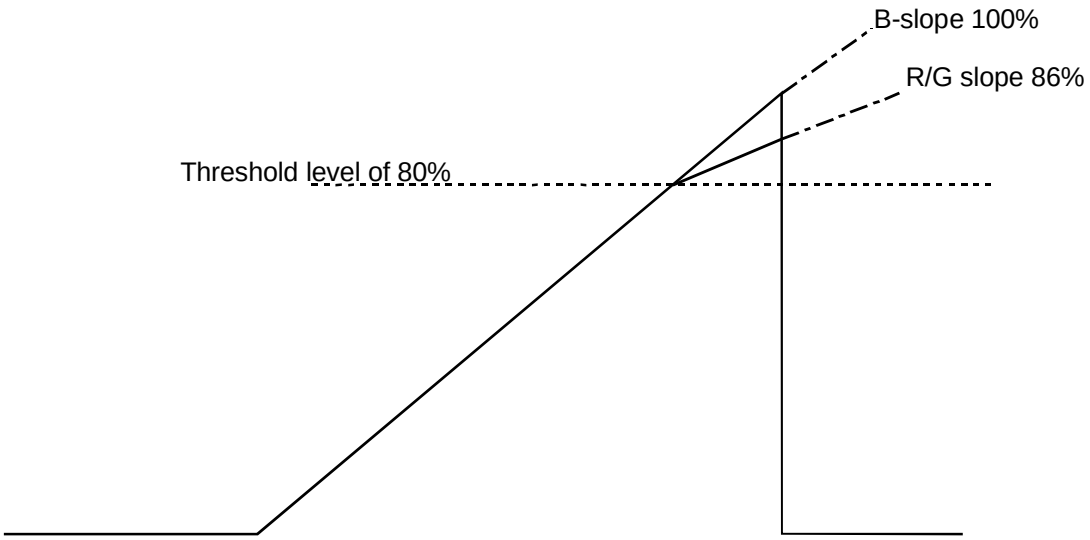


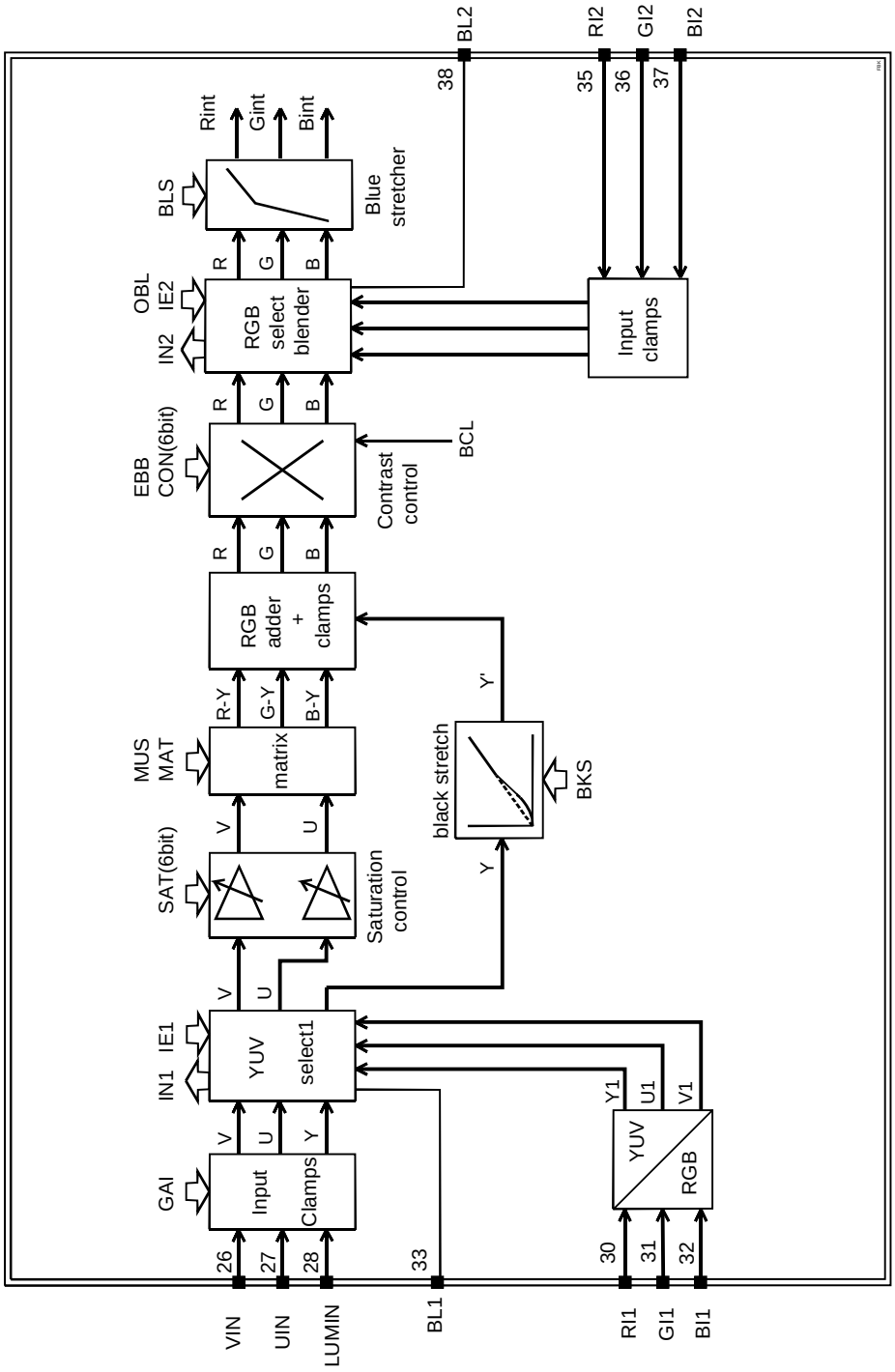
Fig 8 : blue stretcher

When adjusting the white point be sure that the blue stretcher is inactive. In principal all features should be switched off during white point adjustments.

*The second RGB input

This second RGB inputs are specially meant to insert teletext (TXT) or OSD signals.
Before the RGB signal selection the RGB signals are clamped to a similar DC level during burstkey period.
Selection is controlled by the RGB insertion input switch. Fast insertion on the second RGB inputs is made active/inactive via the I²C bus **(IE2)**. With the I^2C bit **IN2** the status of the insertion switch input can be sensed.
Two operating modes can be selected for the fast blanking pin 38 via I^2C bit **OBL**:
- Normal fast RGB insertion 2 ($R2_{IN}$ $G2_{IN}$ $B2_{IN}$) (**OBL** = 0)
- A mixture of both signal sources (the blender function), i.e. $R2_{IN}$, $G2_{IN}$, $B2_{IN}$ with YUV or RGB1 (**OBL** = 1).

The normal fast insertion via the second RGB inputs is similar as described with the first RGB insertion inputs.
If the blender function is selected then the voltage at the second RGB insertion input determines the amount of fading between the internal signal and the second RGB signals. In chapter “Application remarks per functional block and per pin” paragraph “RGB output and input circuit”, pin 38 the blender characteristic is given (Fig 22).
The Blender input has been optimised on the blender output characteristic of the SAA5800 (µprocessor/OSD/teletext processor).



A 3: Block diagram: YUV/RGB processing.

2.2.3.2 RGB-control

On page 43 the block diagram of the RGB-control is given.(see Fig A 4)
- *RGB processing/ output stage
- * Peak White Limiting / softclipper
- *Beam current limiting
- *****RGB-outputs stages
- *Continuous Cathode Calibration (CCC).
- *****Vg2 adjust window
- *Fixed beam current discharge.

*** RGB processing**
The selected RGB signals are via the I²C bus controlled on
-contrast
-brightness
-RGB white-point adjust (one individual control per channel)

Contrast can be adapted over a 20dB gain range (-14 dB to +6 dB) by means of the I²C function: **CONTRAST: 00 --> 63**. Nominal contrast setting (0 dB) is realised with I²C bus setting **CONTRAST = 44**.

For brightness, a change of DC-level of ± 1 V at RGB_{OUTPUT} (w r t nominal) is possible for a change in I²C bus command **(BRIGHTNESS: 00 -> 63)**. For nominal brightness (Brightness=32), the RGB_{OUTPUT} is at black level which is equivalent to a $I_{CATHODE}$ of the CRT of 0mA. At the brightness function control signals used for the continuous cathode calibration circuit are inserted.

For white-point adjustment, a ±3dB change in channel gain is possible for a change in I²C bus commands **(WHITE POINT ADJUSTMENT RGB (WPA R,G,B): 00 -> 63).** Nominal white-point adjustment settings are realised with I²C bus settings **WPA R,G,B = 32**.

***Peak white limiting /softclipper**

The Peak White Limiting (PWL) of the TDA993X is controlled by is the I^2C control register **PWL** , which is a 4 bits register. This PWL function reacts on relative small white areas of the video signal. (for instance on inserted OSD-box). In front of the PWL function a low pass filter is added. The filter capacitor must be externally added, and allows adaptation of the filter characteristic. In order to have the same low pass filter characteristic of the peak white limiting for 1 Fh and a 2 Fh TV-sets the low pass filter is internally adapted to the selected 1 Fh or 2 Fh standard. This prevents that there is a difference between the PWL level 1Fh or 2Fh set.
Under the condition of maximum contrast and a video inputs signal with a small white box , (small such that the average beam current function is not active) the minimum and maximum PWL attack level can be defined as:
-Minimum PWL action (**PWL** setting 15) → 85% of the Y-input signal applied at the input(s) of the TDA933X
-Maximum PWL action (**PWL** setting 00) → 55% of the Y-input signal applied at the input(s) of the TDA933X
Besides a PWL function also a soft clipper is implemented. This soft clipper is only intended to clip high frequency peaks of the video signal. By I^2C bits **SC1,0** the soft clipper level can be adjusted to four levels with respect to the with respect to the peak white limiter level, set by **PWL**. Take notice that there is a small PWL-level change due to the soft clipper action. The soft clipper will reduce high frequency peaks with about 15 dB.

***Beam current limiting**
The beam current limiting circuit or average beam current limiting (ABL) needs external circuitry to function. The voltage applied at the beam current pin must be a reflection of the amount of beam current through the picture tube. This function is a relative slow function and reduces the contrast and brightness of RGB signals.
For the average beam current limiting:
- contrast reduction begins when $V_{BCL} < 3.0V$;
- brightness reduction begins when $V_{BCL} < 2.0V$.

V_{BCL} is normally 3.3V when average beam current limiting (and peak white limiting) are not active.
The contrast and/or brightness reduction of the RGB_{OUT} is proportional to the voltage decrease on the BCL pin.

*** RGB output stages.**

Before discussing the 2-point black current loop stabilisation or continuous cathode calibration loop (CCC-loop) it is perhaps better to discuss the RGB-output stages first. Because besides that at this function the H- and V-blanking are inserted, the DC-levels of the blanking are 0.5V below nominal black level of the video signal, also several DC-levels are inserted at the RGB-outputs. These levels are used as measuring lines for the CCC-loop. (see Fig 9). At the end of the vertical blanking (line 18,19,20,21 for 1 Fh, 50 Hz) the measuring lines for (CCC)loop can be observed The exact position of the measuring lines for various modes can be found in
Fig 5 and Fig 6 in chapter "Vertical synchronisation/deflection and geometry (horizontal & vertical)".
These measuring pulses have three DC-levels:
-A DC-level of -0.1V with respect to nominal black level during the leakage measurement (LO). This level is chosen so that it lies close to the black level in order to have an accurate measurement close to cut off voltage of the picture tube.
-A pulse of +0,25V with respect to nominal black level, which corresponds with a cathode current of 8µA
-A pulse of +0,38V above nominal black level which corresponds with a cathode current of 20µA
The pulse-levels of +0.25V and +0.38V can only be seen measured on alternating fields In the next paragraph CCC-loop will be described

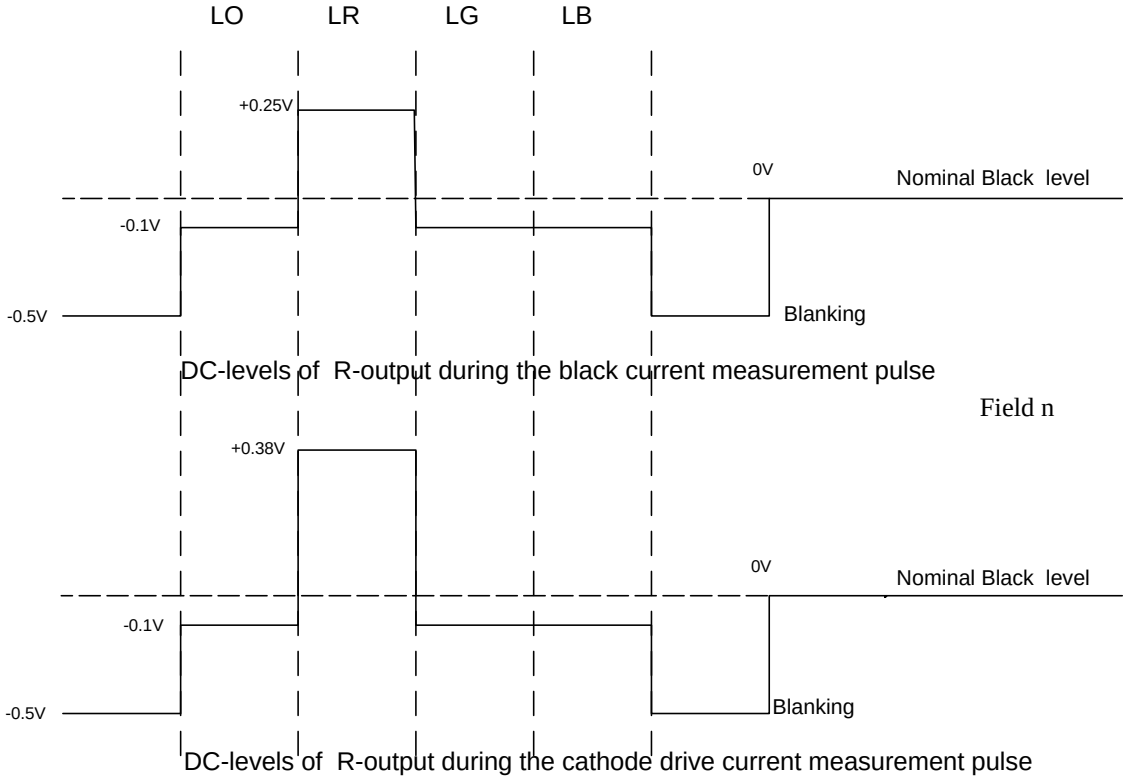


Fig 9 : DC-level at RGB outputs

Important to tell is that the RGB blanking level tracks with the DC level of the black current measurement pulses.
The total video signal (except the measuring pulses for the CCC-loop) can be blanked by activating the I^2C function **RBL** (RGB blanking). The RGB output stages supply the buffered RGB signals to pins 40, 41and 42 respectively.

*** Continuous Cathode Calibration (CCC)**

The Continuous Cathode Calibration (CCC) loop (or two point stabilisation loop) is an auto-tuning loop which stabilises the black level (offset) as well as the cathode drive level (gain) of each gun of the CRT sequentially and independently on alternating fields. The benefit of the CCC-loop can be best explained by the figure below.

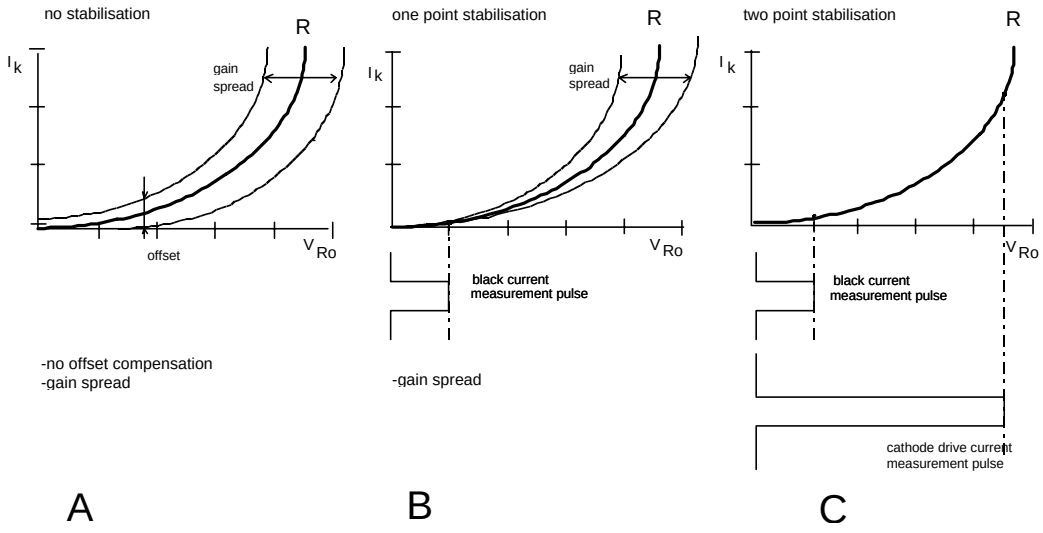


Fig 10 : CCC-loop correction mechanisms

The graphs show the cathode current (I_K) as function of one of the three video output signals (in this case the red output) of the TDA933x.
In case of no stabilisation, the transfer characteristic changes as function of temperature and ageing of the tube. This results in an offset and gain error , see graph A. An one point stabilisation corrects for offset variations (graph B) however with the CCC-loop both offset and gain spread are compensated as given in graph C.

The CCC-loop can be divided into two loops:
-a black level stabilisation loop (cut -off compensation)
-a cathode drive stabilisation loop. (gain compensation)

Besides these two loops a leakage current compensation loop is present.
This loop compensates the total offset current of the three cathodes of the picture tube and the offset of the three RGB-amplifiers. The leakage current compensation range is about ±100µA. Leakage measurement and compensation occurs every field.

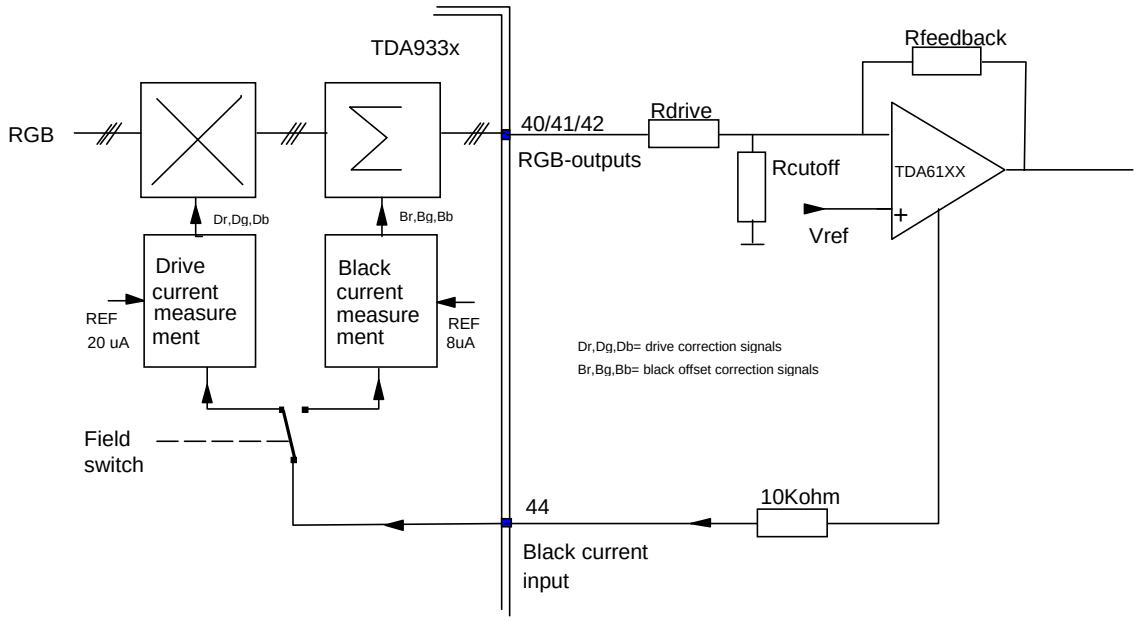


Fig 11 : Basic application of the CCC-loop with the TDA61XX

In Fig 11 basic application of the CCC-loop with RGB amplifiers is given.
In this figure the main two loops of black level stabilisation and cathode drive stabilisation are shown.
The two loops are being stabilised on alternating fields by means of a field switch.

The main difference of the two loops is:
During black level stabilisation internal black level clamps ensure that the DC-levels at RGB-outputs are independently and sequentially changed so that always 8µA flows to the black current input (pin 44). during the 3 measurement lines (LR,LG,LB) for the black current offset levels. The black current offset correction signals are stored internally.
During the cathode drive current stabilisation, internal multipliers ensure that the cathode drive level for the three guns of the CRT are independently and sequentially stabilised so that 20µA feedback current flows to the black current input (pin 44) during the 3 measurement lines (LR,LG,LB) for the drive levels. The correction for the drive signals are stored internally.

The drive levels at the three cathodes of the tube are always adjusted by the CCC-loop such that the feedback current is 20µA This means that the gain of the RGB-amplifier, e.g. TDA61XX family, is NOT determining the drive level to the CRT anymore. In order to change the cathode levels at the picture tube four I^2C bits are added **CL3..0**

Changing the cathode level at the picture tube is achieved in the following way:
The **CL3..0** bits vary the amplitude of the RGB channels together of the internal measurement lines generated in a programmable pulse generator. During the 3 measurement lines (LR,LG,LB) these levels are inserted on the RGB video signals.

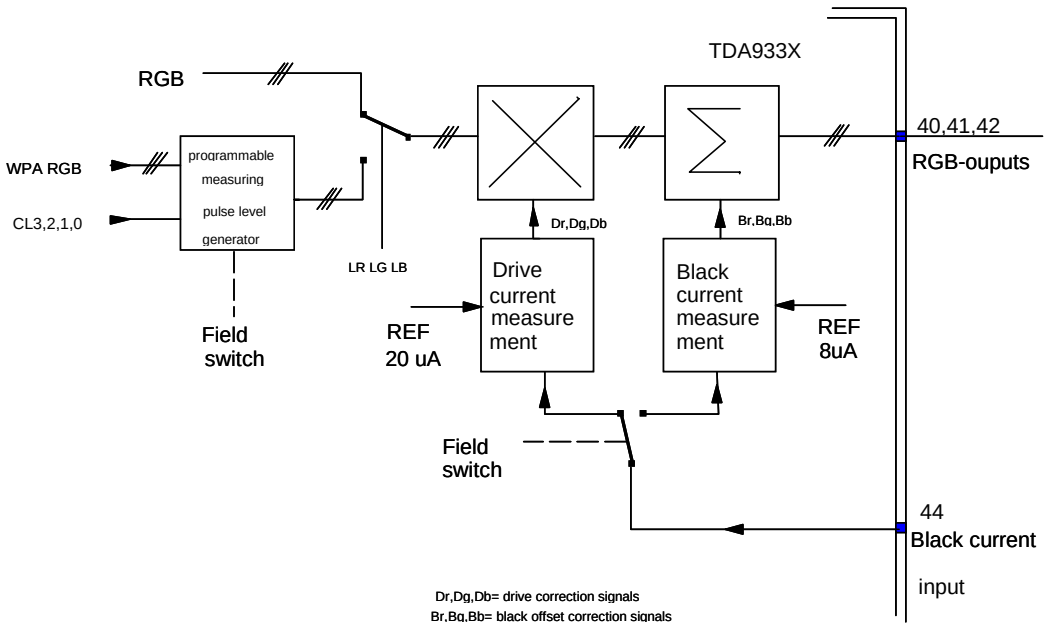


Fig 12 : Main blocks of the CCC-loop

The drive correction signals (Dr, Dg, Db) will change the gain of the multipliers such that internal generated measurement pulse give a drive current measurement line at the cathode of the CRT corresponding with a current of 20µA. This 20µA current will be fed back to the black current input pin 44.
The drive correction signals(Dr,Dg,Db) will be stored internally so that, after the 3 measurement-lines(LR,LG,LB), the actual RGB-video signals will have the same multiplication factor as determined during the drive current measurement pulses.
The same procedure takes place during black current measurement except now the measurement lines are adapted such that a 8µA cathode current is measured by adding the offset correction signals (Br, Bg , Bb) to the RGB-signals By means of the field switch the programmable measurement line level generator switches the internal measurement line level corresponding with a 20µA cathode to a internal level corresponding with a 8µA cathode current.
The field switch is not synchronised with odd / even fields.

Changing the WPA RGB registers works on the same way as changing the **CL3..0** bits except this three registers react on each individual RGB signal where the **CL3..0** bits react on all three RGB-signals together.
So when changing the WPA RGB registers the internal generated measurement lines are adapted at the input of the CCC-multiplier the CCC-loop adjust itself so that the black current measurement lines at the black current input (pin 44) are constant (8µA and 20µA).

Start up behaviour of the CCC-loop.

After H-out is released the RGB-outputs are blanked and the CCC-loop is direct active, so from the start the 250mV and 380mV measuring pulses are present at the RGB-outputs. The cathodes of the picture tube are driven by the 250mV and 380mV measuring lines but due to the fact that the tube is cold (heater voltage is just applied, emission is very low) the corresponding 8µA and 20µA are not measured at the black current input so the gain as well as the offset is set to maximum by the CCC-loop what results in the fact that the CCC-loop gets out of range. This means that the amplitude of the 3 measuring lines is maximum at the RGB outputs. (actual scan remains at blanking level). After 7 to 15 seconds, the heater has warmed up the cathodes to generate enough emission. At that moment the CCC-loop starts to measure 8µA and 20µA at the black current input pin and at the same time the I^2C Black current loop failure sense bit **BCF** becomes zero, at which moment the RGB-outputs will be released.

For applications without a picture tube the CCC-loop can be switched off by means of the I^2C control bit **AKB** (**A**uto **K**ine **B**iasing). In case **AKB** is switched off the RGB blanking and **WPA R,G,B** registers are disabled.

In principal there is no difference in working for the CCC-loop in 1 Fh or 2 Fh mode. In both modes, the three measuring lines R, G and B are generated, each lasting one line period. (See Fig 9, page 37) Each alternate field the cut-off level (8 µA) or the drive level (20 µA) is measured and adjusted. The only difference is the timing of the internal measurement window of loop.
For 1 Fh applications the measurement window starts at 50% of the measuring line and stops at 75% of the line. The measurement windows duration is 16µs
For 2 Fh applications the measurement window starts 25% of the measuring line and stops at 75% of the line So the measurement window duration is also 16µs. Since the measuring window duration in 1 Fh and 2 Fh is equal all internal time constants of the CCC-loop are not dependent on 1 Fh or 2 Fh mode.

***VG2 window**
Via the I^2C bus VG2 can be aligned in production. The TDA933X measures automatically the DC-level of the measuring lines of the cut-off loop of the CCC-loop.
Internal, a window is defined of 2.5 Volt ± 100 mV. By turning the VG2 potentiometer the DC-level at the RGB-output will change. Whenever the lowest DC-level of the three RGB-outputs is within this window the VG2 is correctly aligned. Note that the lowest RGB output corresponds with the highest cut-off level at the cathode of the picture tube. “Within window” can be read back with the I^2C output bit **WBC.** With the **HBC**-bit can be monitored whether the DC-level is above or below this window.
The only restriction on this alignment method is that the VG2 window is fixed at a DC-level of 2.5V ±100mV. This implies that the RGB amplifiers should be designed to have the required highest (raster) cut-off level at their outputs at 2.5 Volt DC input level. The raster cut-off level is 10 - 12 Volt lower than the usual specified spot cut-off level.

***Fixed beam current discharge**
This function " fixed beam current switch off" is used to discharge EHT voltage of picture tubes without bleeder when switching to standby or switching off the power supply. By means of the IIC function "**F**ixed **B**eam **C**urrent switch off" **FBC**=1 this function can be enabled. In combination with the IIC function Switch Off in vertical Overscan (bit **OSO**) can be determined whether the set is discharged in vertical overscan or during normal scan. There is in difference in behaviour of this function between switching to standby and switching off the power supply using the mains switch. So has pin 29 no function when the set is switched to standby (**STB1,0**).
Therefore the function will be explained below for both switching off the power supply using the mains switch and for switching to stand-by using **STB1,0**.

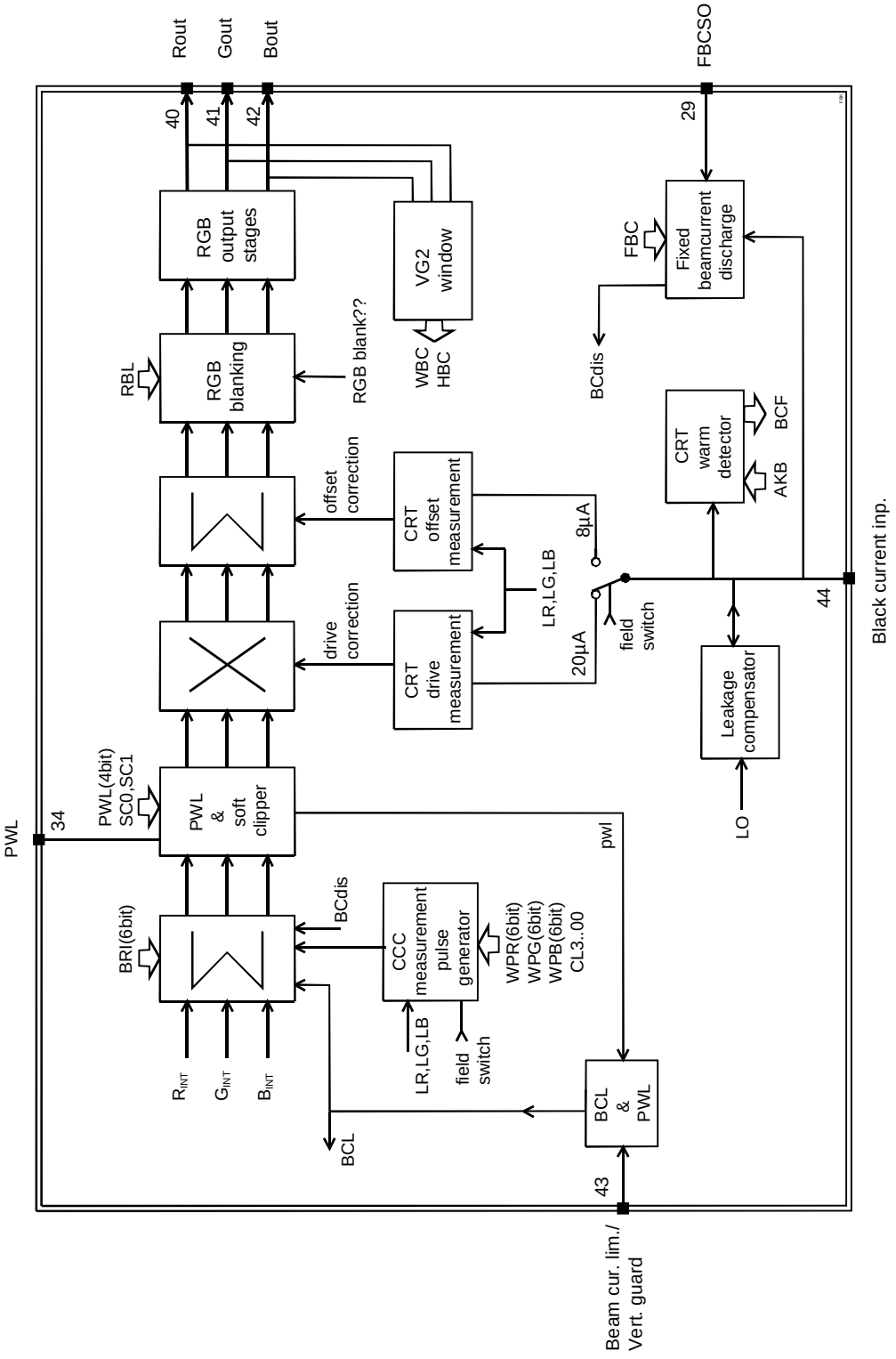
Switching the power supply off using the mains switch:
The power supply (the deflection supply) is "sensed" with an external circuit. The status of the power supply is fed to pin 29. A voltage below the 1.5V at this pin 29 means the supply works normally. When the supply voltage drops, pin 29 should be pulled above 1.5 Volt. This activates the fixed beam current function (provided bit **FBC**=1) and the following procedure is started:

- The vertical scan is completed and vertical flyback is made
- Inside pin 44 "the black current input" a current measurement of 1mA is activated. This current is adjusted and kept at 1 mA by adapting the brightness level of the RGB outputs. In other words: the brightness control discharges the tube, the discharge current of 1mA is measured via the black current input pin 44.
- The discharge takes place during the overscan when **OSO** bit =1 which minimises the visability of the discharge on the screen of the picture tube.
- The discharge begins when the voltage at pin 29 becomes high and ends when the supply voltage of the TDA933X drops below the power on reset level (about 6.2V). When a power on reset is detected both H-out and the discharge current are disabled.

Switching to stand-by using **STB1,0**:
When switching the IC to Standby mode also discharge of the EHT voltage can take place when **FBC**=1.
The procedure is the same as above (including the use of **OSO**) except:

- Pin 29 has no function
- A slow stop is made by the horizontal output. This means that the T-on of H-out decreases linear from nominal to zero in 43msec During the first 38ms of the slow stop time the fixed beam current switch off is activated in order to discharge the EHT voltage.

See also chapter “Horizontal synchronisation”, paragraph “H-output and slow start/stop”



A 4: Block diagram: RGB-processing and control.

2.2.4 I²C bus description

2.2.4.1 Overview I²C bits

For easy control, most functions of the TDA933X are controlled via the I²C bus:

Input functions[1] (write)		Sub addr. (hex)	Data bits							
			D7	D6	D5	D4	D3	D2	D1	D0
RGB processing-1		00	MAT	EBB	SBL	RBL	BLS	BKS	IE1	IE2
RGB processing-2		01	MUS	FBC	OBL	AKB	CL3	CL2	CL1	CL0
Wide horizontal blanking		02	HBL	0	GAI	STB0	HB3	HB2	HB1	HB0
Horizontal deflection		03	0	VSR	FAST	STB1	POC	PRD	VGA[2]	ESS
Vertical deflection		04	0	VFF	LBM	DIP	OSO	SVF	EVG	DL
Brightness	BRI	05	0	0	A5	A4	A3	A2	A1	A0
Saturation	SAT	06	0	0	A5	A4	A3	A2	A1	A0
Contrast	CON	07	0	0	A5	A4	A3	A2	A1	A0
White point Red	WPR	08	0	0	A5	A4	A3	A2	A1	A0
White point Green	WPG	09	0	0	A5	A4	A3	A2	A1	A0
White point Blue	WPB	0A	0	0	A5	A4	A3	A2	A1	A0
Peak White Limiting	PWL	0B	0	0	SC1	SC0	A3	A2	A1	A0
Horizontal Shift	HSH	0C	0	0	A5	A4	A3	A2	A1	A0
Horizontal Parallelogram	HP	0D	0	0	A5	A4	A3	A2	A1	A0
E-W amplitude	EW	0E	0	0	A5	A4	A3	A2	A1	A0
E-W parabola/width	PW	0F	0	0	A5	A4	A3	A2	A1	A0
E-W corner parabola	CP	10	0	0	A5	A4	A3	A2	A1	A0
E-W trapezium	TC	11	0	0	A5	A4	A3	A2	A1	A0
E-W EHT hor.comp.sens.	HCS	12	0	0	A5	A4	A3	A2	A1	A0
Vertical slope	VS	13	0	0	A5	A4	A3	A2	A1	A0
Vertical amplitude	VA	14	0	0	A5	A4	A3	A2	A1	A0
S-correction	SC	15	0	0	A5	A4	A3	A2	A1	A0
Vertical shift	VSH	16	0	0	A5	A4	A3	A2	A1	A0
Vertical Zoom	VX	17	0	0	A5	A4	A3	A2	A1	A0
Vertical Scroll	VSC	18	0	0	A5	A4	A3	A2	A1	A0
Vertical Wait	VWT	19	0	0	0	A4	A3	A2	A1	A0
DAC output [3]	DAC	1A	0	0	A5	A4	A3	A2	A1	A0
Output (read)			Data bits							
Status byte 0		00	POR	FSI	SL	XPR	NDF	IN1	IN2	WBC
Status byte 1		01	ID3	ID2	ID1	ID0	NHF	BCF	FLS	NRF
Status byte 2		02	X	X	X	X	X	X	X	HBC

Table 4 : Condition PHI-1 loop

1) Note: All not-used bits should be set to zero, for compatibility with future devices.
2) Only available for TDA 9331 and 9332
3) Only available for TDA 9330 and 9332, for TDA9331 the DAC output is proportional to the horizontal frequency in VGA mode and set to minimal in TV mode.

For quick reference are all bits listed in alphabetical order in the two tables below. The bits are split up for control functions and analogue control.:
The meaning of the different columns in the table are:

Control bits table:

CONTROL BIT	The short name for the control bit
FUNCTION	A short functional description
REG	The register subadress in HEX.
BIT	The bit number (D7..D0) in the register
I/O	Input or Output, Input = control bit, Output = status bit
MACRO	The device macro, where the bit is related to: Sync: Horizontal and Vertical synchronisation Geo: Geometry (vertical & horizontal) and drive of vertical deflection RGB: RGB output, input and control Pow/Prot: Power and Protection control Idselect Type number identification
FU	Function class, the bits are divided in 5 classes: SU **S**tart-**U**p, bit has to be set correct before switching on from stand-by. AL **Al**ignment, bit(s) have to be aligned during production, the found values are set each time before switching on from stand-by SC **S**etmaker **C**ontrol, bits which have to be controlled by the setmaker during operation for correct performance like PHI-l loop time constant, positive modulation, etc. UC **U**ser **C**ontrol, bits which are normally accessible for the customer like contrast, brightness, etc.

Analogue control:
Most columns are identical. The deviating columns:

STEPS	The number of steps, available for this analogue function
RANGE	The control range of the analogue control.

Alphabetic list of I2C control bits.

CONTROL BIT	FUNCTION	REG	BIT	I/O	MACRO	FU
AKB	**A**uto **K**ine **B**iasing, 0=enable black current stabilisation loop, 1=disable	02	4	I	RGB	SU
BCF	**B**lack **C**urrent loop **F**ailure, 1=loop is not stabilised	01	2	O	RGB	SU
BKS	**B**lac**K** **S**tretch mode, 1=on	00	2	I	RGB	UC
BLS	**Bl**ue **S**tretch mode, 1=on	00	3	I	RGB	SC
DIP	**D**e-**I**nterlace **P**hase, 0=delay 1st field 0.5 line (reference=V_D) 1=delay 2nd field 0.5 line	04	4	I	Sync	SC
DL	**D**e-inter**L**ace, 1=de-interlace	04	0	I	Sync	SC
EBB	**E**nable **B**lue **B**ack, 1=enable	00	6	I	RGB	SC
ESS	**E**xtended **S**oft **S**tart, 0=normal, 1=extended from 75-100%	03	0	I	Sync	SU
EVG	**E**nable **V**ertical **G**uard, 1=protection enabled	04	1	I	Pow/Prot	SU
FAST	**FAST** acquisition loop (“PHI-1”), 0=normal, 1=increased with 30%	03	5	I	Sync	SC
FBC	**F**ixed **B**eam **C**urrent switch-off, 0=switch-off with blanked RGB outputs, 1=switch-off with fixed beam current	01	6	I	RGB	SC

CONTROL BIT	FUNCTION	REG	BIT	I/O	MACRO	FU
FLS	**FL**a**S**h-over indication, 1=flash-over detected	01	1	O	Pow/Prot	SC
FSI	**F**ield **S**ynchronisation **I**ndication, 0=50/100Hz, 1=60/120Hz	00	6	O	Geo	SC
GAI	**GAI**n Y-input pin 28, 0 = normal (1 V bl-wh), 1 = high (0.32 V bl-wh)	02	5	I	RGB	SU
HBC	**H**elp above/below **B**lack **C**urrent loop window (see WBC), 0=below window, 1=above window	02	0	O	RGB	AL
HBL	**H**orizontal **Bl**anking, 1=extended blanking on for display 4:3 on 16:9 tube	02	7	I	Sync	SC
ID3..0	Device **Id**entification code	01	7..4	O	DevSel	SC
IE1 / IE2	**I**nsertion **E**nable fast blanking, input **1**, **2**, 1=enabled	00	1,0	I	RGB	SC
IN1	Reflects the level on the fast blanking **IN**put pin 33 of RGB**1** 0=low, 1=pin active (RGB insertion)	00	2	O	RGB	SC
IN2	Reflects the level on the fast blanking **IN**put pin 38 of RGB**2** 0=low, 1=pin active (RGB insertion)	00	1	O	RGB	SC
LBM	**L**ong **B**lanking **M**ode, 0=auto, 1=50 Hz blanking	04	5	I	Sync	SU
MAT	PAL/NTSC **MAT**rix, 0=PAL, 1=NTSC matrix	00	7	I	RGB	SC
MUS	NTSC **M**atrix **US**A, 0=Japanese NTSC matrix, 1=USA NTSC matrix	01	7	I	RGB	SC
NDF	**N**o vertical **D**e**F**lection guard output, 1=failure	00	3	O	Pow/Prot	SC
NHF	**N**o **H**orizontal **F**lyback pulse present, 1=failure	01	3	O	Pow/Prot	SC
NRF	**N**o **R**e**F**erence, 1=reference oscill. not locked to X-tal oscill	01	0	O	Pow/Prot	SC
OBL	**O**SD **BL**ending function of BL2 pin 38 from RGB2, 0=normal fast blanking for OSD, 1=blending for OSD	01	5	I	RGB	SU
OSO	**O**verscan **S**witch **O**ff, 1=switch off in vertical overscan	04	3	I	Geo	SU
POC	**P**hi-**O**ne **C**ontrol synchronisation mode, 1=loop switched off	00	3	I	Sync	SC
POR	**P**ower **O**n **R**eset, 1=failure detected	00	7	O	Pow/Prot	SC
PRD	Over-voltage **Pr**otection **D**etection mode, 0=detection, 1=detection & slow stop H-out	03	2	I	Pow/Prot	SU
RBL	**R**GB **BL**anking, 1=outputs blanked	00	4	I	RGB	SC
SBL	**S**ervice **BL**anking, 1=active	00	5	I	Geo	AL
SC1..0	**S**oft **C**lipping level > peak white limiting level, 00=0%, 01=5%, 10=10%, 11=soft clipping off	0B	5,4	I	RGB	SC
SL	**S**ync in **L**ock, 1=acquisition-loop (“PHI-1”) locked	00	5	O	Sync	SC
STB1,0	**ST**and-**B**y control, 00=stand-by, 11=on, 01,10=no action	02 03	4 4	I	Pow/Prot	SC
SVF	**S**et **V**ertical **F**requency, 0=50/60 Hz, 1=100/120 Hz	04	2	I	Geo	SC
VFF	**V**ertical **F**ree running **F**requency, 0=50/100Hz, 1=60/120Hz	04	6	I	Geo	SC
VSR	**V**ertical **S**can **R**eference, 0=falling edge V_D pulse, 1=rising edge V_D pulse	03	6	I	Geo	SU
VGA	**VGA** mode, 0=Fh fixed by internal reference, 1=multi-sync function switched on	03	1	I	Sync	SC
WBC	**W**indow **B**lack **C**urrent loop, 1=within window	00	0	O	RGB	AL
XPR	**X**-ray **PR**otection, 1=failure detected	00	3	O	Pow/Prot	SC

Alphabetic listing of analogue I2C controls. The parameters in the table below are just rough indications and may change without notice. Please consult the TDA933X data sheet (ref.[1]) for the most up-to-date values.

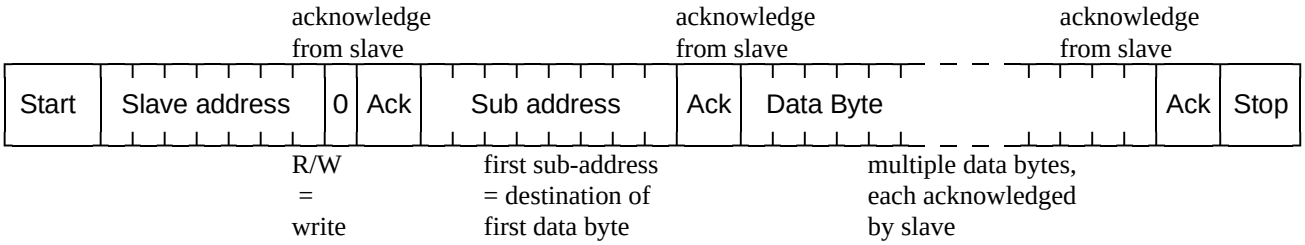
CONTROL BITS	FUNCTION	REG	BIT	STEPS	RANGE	MACRO	FU
BRI	**BRI**ghtness	05	5..0	63	- 1 .. + 1 V[1)]	RGB	UC
CL3..0	**C**athode drive **L**evel, adjustment cathode drive amplitude	01	3,2,1,0	16	50 .. 95 V_{Bl-Wh}	RGB	AL
CON	**CON**trast	07	5..0	63	10 ..100 % (20dB)	RGB	UC
CP	E_W **C**orner/**P**arabola	10	5..0	63	-43 .. 0 %	Geo	AL
DAC	**D**ig/**A**nal. **C**onv. Output	1A	5..0	63	0.3 .. 4.0 V	Sync	SC
EW	**E**-W **W**idth	OE	5..0	63	100 .. 65 %	Geo	AL
HB3..0	**H**orizontal **B**lanking position	02	3..0	16	-2.03..+2.03 µs (1Fh) -1.01..+1.01 µs (2Fh)	Sync	
HCS	**H**orizont.**C**ompensation **S**ensitivity	12	5..0	63	0 .. 9 %/V	Geo	SU
HP	**H**oriz. **P**arallelogram	0D	5..0	63	-0.54..+0.54 µs (1Fh) -0.27..+0.27 µs (2Fh)	Sync	AL
HSH	**H**orizontal **S**hift	0C	5..0	63	-4.5 .. +4.5 µs (1Fh) -2.25..+2.25 µs (2Fh)	Sync	AL
PW	E-W **P**arabola/**W**idth	0F	5..0	63	0 .. 22 %	Geo	AL
PWL	**P**eak **W**hite **L**imiting	0B	3..0	16	0.55 .. 0.85 V_{Bl-Wh} Y	RGB	SC
SAT	**SAT**uration	06	5..0	63	0 .. 300 %	RGB	UC
SC	**S**-**C**orrection	15	5..0	63	0 .. 30 %	Geo	AL
TC	E-W **T**rapezium **C**orr.	11	5..0	63	-5 .. +5 %	Geo	AL
VA	**V**ertical **A**mplitude	14	5..0	63	80 .. 120 %[2)]	Geo	AL
VS	**V**ertical **S**lope	13	5..0	63	-20 .. +20 %	Geo	AL
VSC	**V**ertical **Sc**roll	18	5..0	63	-18 .. +19 %	Geo	UC
VSH	**V**ertical **Sh**ift	16	5..0	63	-5 .. +5 %	Geo	AL
VWT	**V**ertical **W**ai**T**	19	4..0	23[3)]	8 .. 31 lines	Geo	SU
VX	**V**ertical zoom/e**X**pand	17	5..0	63[4)]	75 .. 138 %	Geo	UC
WPR,G,B	**W**hite **P**oint **R**,**G** and **B**	08,09,0A	5..0	63	-50 .. +50 %[5)]	RGB	AL

Note:
1) Relative variation with respect to the measuring pulses at RGB_{OUT}.
2) Valid when $SC=00_{HEX}$, for $SC=3F_{HEX}$ the range is 86 .. 112%.
3) 00 - 08 $_{HEX}$ have default 8 lines delay, 09 - 1F $_{HEX}$ from 9 - 31 lines delay
4) Neutral position for VX is $19_{HEX} = 25_{DEC}$.
5) Nominal setting=$1F_{HEX}$.

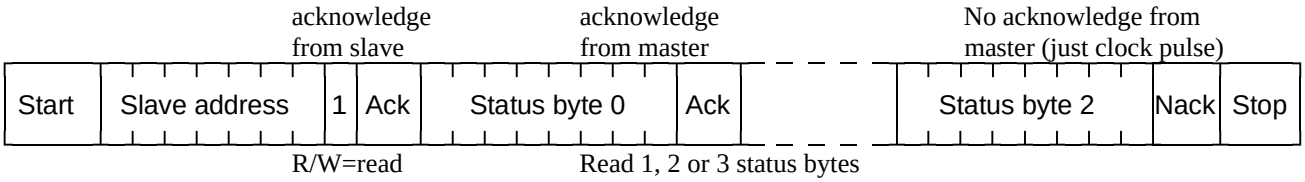
The TDA933X needs only two I²C-bus pins (10=SCL and 11=SDA) to read and write all its functions:

- Write slave address: $8C_{HEX}$: A6 A5 A4 A3 A2 A1 A0 R/W : 1 0 0 0 1 1 0 0
- Read slave address: $8D_{HEX}$: A6 A5 A4 A3 A2 A1 A0 R/W : 1 0 0 0 1 1 0 1

For I²C-bus write-transmissions the TDA933X has automatic sub-address increment, so multiple data bytes can be sent in one transmission.



Reading the three status bytes is done **without sub-addressing**. After receiving the I²C-bus read address, the TDA933X always starts with status byte 0.



2.2.4.2 I²C-bus start-up procedure.

The TDA933X has many alignment-free internal circuits that are calibrated with the frequency of the reference Xtal oscillator. To ensure correct register content at start-up, the following start-up procedure should be implemented in the software:

- •1 Keep reading the I²C-bus status bytes, until **POR** = 0
- •2 Set **STB1,0** = 0 0
- •3 Write all subadresses up till including $1A_{HEX}$
- •4 Keep reading I^2C-bus status bytes till **NRF** = 0
- •5 Set **STB1,0** = 1 1

Before the horizontal drive output can become active, all sub-address bytes 00_{HEX} to $1A_{HEX}$ must be loaded. Registers or register bits, not available or defined in certain versions, must be loaded with zero's for (future) compatibility. After the last sub-address is loaded, the oscillator is calibrated. After successful calibration, **NRF** is set 0.

Each time before the sub-address bytes are refreshed, the status bytes must be read. If **POR**=1 then the start-up procedure must be carried out to restart the IC. Not following this procedure may result in undesired conditions after power-up or a power dip (e.g. incorrect horizontal line frequency).

The following paragraphs describes the function of the I^2C control bits.
Mentioned pin numbers refer to the QFP package.

2.2.4.3 Synchronisation part.

Input control bits

DIP : **D**e-**I**nterlace **P**hase Reg: 04 Bit: 4 Fu: SC
When using de-interlacing (see **DL** below) with **DIP** the field can be selected which is delayed for 0.5 line. The vertical input pulse V_D serves as reference. In this way, a wide variety of TXT processors can be interfaced.
0 = delay first field with 0.5 line
1 = delay second field with 0.5 line

DL : **D**e-inter**L**ace Reg: 04 Bit: 0 Fu: SC
This can switch off the interlace, e.g. for TEXT applications.
0 = Interlace
1 = De-interlace

ESS : **E**xtended **S**oft **S**tart Reg: 03 Bit: 0 Fu: SU
The soft start gradually increases the "on"- time of the horizontal drive from 0 % to 52 % while the "off" time is kept fixed on 48 % (percentages related to the dutycycle in final situation). The EHT will be proportional to the horizontal drive frequency. To prevent flash-over in certain picture tubes, it is best to have a low speed EHT build-up from 75% to 100%. This can be achieved by slowing down the "on" - time increase during the last part.
0 = normal "on"-time increase (156 ms)
1 = normal "on"-time increase to 39% (120 ms), slow increase to 52% (1030 ms)

FAST : **FAST** acquisition loop time constant Reg: 03 Bit: 5 Fu: SC
The acquisition loop ("PHI-1") time constant is integrated. For flexibility, the speed can be increased by 30% for quick settling of H_D disturbances (pending on applied scan converter, applied input processor and/or input source e.g. VCR).
0 = Normal time constant
1 = Loop speed increased with 30 %

HBL : Wider **H**orizontal **Bl**anking Reg: 02 Bit: 7 Fu: SC
Widens the horizontal blanking for well defined edges with underscan.
0 = Normal blanking using horizontal flyback pulse
1 = Wider blanking to obtain well defined left and right edges e.g. for 4:3 picture and 16:9 screen size.

LBM : **L**ong **B**lanking **M**ode Reg: 04 Bit: 5 Fu: SU
This bit sets the 60 Hz vertical blanking interval to the 50 Hz standard. In certain 50/60 Hz applications this can simplify the vertical output stages, regarding the maximum vertical retrace time. With a fixed 50 Hz blanking time, visible vertical retrace lines with 60 Hz can be avoided when the vertical retrace time is too long (> 1 ms). **LBM** is only working in 1 Fh mode!
0 = Blanking adapted to standard (50 or 60 Hz)
1 = Fixed blanking according 50 Hz standard

POC : "**P**hi-**O**ne" (acquisition loop) **C**ontrol Reg: 00 Bit: 3 Fu: SC
When this bit is switched to high, the acquisition-loop is switched off completely. In this mode very stable OSD or TEXT can be displayed, independent of the selected source. Useful for e.g. installation menu's, blue mute. It is also possible to measure the free running frequency in this way.
Note: if **POC**=1 than **SL** =0
0 = Synchronisation active
1 = Synchronisation not active

VGA : **V**ideo **G**raphics **A**dapter mode Reg: 03 Bit: 1 Fu: SC
In normal mode, horizontal and vertical deflection are optimised for displaying signals related to the TV-norm.
In VGA mode, the horizontal frequency range is increased (15 to 25 kHz 1Fh, 30 to 50 kHz 2Fh), the allowed number/lines per field is adapted and the vertical amplitude is kept constant independent of the vertical frequency.
(Bit only available in TDA 9331/2)
0 = normal mode
1 = VGA mode

Output control bit:

SL : **S**ync **L**ock Reg: 00 Bit: 5 Fu: SC
Lock indication of acquisition loop ("Phi-1") to incoming H_D pulse:
0 = Not locked
1 = Locked to the incoming H_D pulse

Analogue controls:

DAC: **D**igital to **A**nalogue **C**onvertor output Reg: 1A Bit: 5..0 Fu: SC
This general purpose DAC output can be used for alignment or other DC controlled functions. (only available in TDA 9330/2)
Nr. of steps: 63
Range: 0.3 .. 4.0 Volt

HB3..0: Wide **H**orizontal **B**lanking position Reg: 02 Bit: 3..0 Fu: AL
When switching on the wide horizontal blanking using **HBL**, the exact position of the edges can be adjusted with **HB3..0**.
Nr. of steps: 16
Range: - 2.03 .. +2.03 µs (1 Fh)
- 1.015 .. +1.015 µs (2 Fh)

HP: **H**orizontal **P**arallelogram correction Reg: 0D Bit: 5..0 Fu: SC
When the horizontal and vertical deflection yokes are not orthogonal, the vertical lines can be set in correct position.
Neutral position: 1F HEX
Nr. of steps: 63
Range: - 0.54 .. + 0.54 µs (1 Fh mode)
- 0.27 .. + 0.27 µs (2 Fh mode)

HSH: **H**orizontal **Sh**ift Reg: 0C Bit: 5..0 Fu: AL
Adjusts the horizontal position of the picture on the screen
Nr. of steps: 63
Range: - 4.5 .. + 4.5 µs (1 Fh mode)
- 2.25 .. + 2.25 µs (2 Fh mode)

2.2.4.4 Geometry

Input control bits:

OSO : **O**verscan **S**witch-**O**ff Reg: 04 Bit: 3 Fu: SU

Enable switch-off in vertical overscan. When switching to stand-by, the vertical deflection is kept high while during switch-off the picture tube is discharged with a fixed current so the white drive is less visible

0 = Switch-off undefined
1 = Enable switch-off in vertical overscan function

SBL : **S**ervice **Bl**anking Reg: 00 Bit: 5 Fu: AL

This bit blanks the bottom half of the picture, starting exactly in the middle of the vertical scan (deflection currents are zero). This bit is intended be used to align the vertical parameter **VS** in order to compensate for component tolerances. See also the chapter about geometry alignment.

0 = No service blanking
1 = Service blanking active

SVF : **S**et **V**ertical **F**requency Reg: 04 Bit: 2 Fu: SU

To control the vertical free running frequency independent from the horizontal frequency (1Fh or 2 Fh) the vertical frequency can be set to 1 Fv (50/60 Hz) or 2 Fv (100/120 Hz). In this way, also progressive scan can be easily applied. The vertical free running frequency (50/100 or 60/120 Hz) can be set using **VFF** (see below).

0 = 50 / 60 Hz
1 = 100 / 120 Hz

VFF : **V**ertical **F**ree running **F**requency Reg: 04 Bit: 6 Fu: SC

The vertical free running frequency can be set to 50/100 Hz or 60/120 Hz. The selection between 1 Fv (50/60 Hz) and 2 Fv (100/120 Hz) can be made using **SVF** (see above).

0 = 50/100 Hz
1 = 60/120 Hz

VSR : **V**ertical **S**can **R**eference Reg: 03 Bit: 6 Fu: SU

It is possible to select whether the rising or falling edge from the V_D pulse is used for the vertical reference. This increases the flexibility to interface with a variety of scan converters or picture improvement circuits.

0 = Falling edge V_D pulse is vertical scan reference
1 = Rising edge V_D pulse is vertical scan reference

Output control bit:

FSI : **F**ield **S**ynchronisation **I**nformation Reg: 00 Bit: 6 Fu: SC

Indication of the field frequency of theV_D pulse. Not valid in VGA mode. 1 Fv (50/60 Hz) or 2 Fv (100/120 Hz) is determined by the setting of **SVF** (see above)

0 = 50/100 Hz
1 = 60/120 Hz

Analogue controls:

CP: E-W **C**orner **P**arabola Reg: 10 Bit: 5..0 Fu: AL
Adjusts the top- and bottom curve of the vertical lines.
Set **CP** in neutral position before starting alignment.
Neutral position: 1F HEX.
Nr. of steps: 63
Range: -21.5..+21.5 % (related to neutral position $1F_{HEX}$, -43 .. 0 % related to 00_{HEX})

EW: **E**-W **W**idth Reg: 0E Bit: 5..0 Fu: AL
Adjusts the picture width. When all higher order terms (**CP, PW, TC**) are aligned, the geometry corrections will remain correct when changing the **EW** register for horizontal zoom.
Nr. of steps: 63
Range: 65 .. 100 %

HCS : **H**orizontal **C**ompensation **S**ensitivity Reg: 12 Bit: 5..0 Fu: SU
Sets the EHT tracking sensitivity to modulate the E-W width using the information on pin 4. EHT tracking compensates picture size variations due to beam current variation. The vertical EHT tracking sensitivity is fixed (9 %/V). The circuit interfacing pin 4 should be designed for correct compensation of the vertical amplitude, the horizontal compensation can be matched using **HCS**.
Nr. of steps: 63
Range: 0 .. 9 %/V

PW: E-W **P**arabola **W**idth Reg: 0F Bit: 5..0 Fu: AL
Adjusts the parabola correction.
Nr. of steps: 63
Range: 0 .. 22 %

SC: Vertical **S**-**C**orrection Reg: 15 Bit: 5..0 Fu: AL
Adjusts the vertical S-correction.
Nr. of steps: 63
Range: 0 .. 30 %

TC: E-W **T**rapezium **C**orrection Reg: 11 Bit: 5..0 Fu: AL
Adjusts the position of the vertical lines at the sides: can be bend inwards or outwards. The vertical lines remain straight.
Set in neutral position before starting alignment.
Neutral position: 1F HEX
Nr. of steps: 63
Range: -5 .. +5 %

VA: **V**ertical **A**mplitude Reg: 14 Bit: 5..0 Fu: AL
Adjusts vertical amplitude. Adjustment does affect all horizontal geometry corrections and also the vertical S-correction. Before using **VA**, first align **VS** and **VSH**.
Do not use for vertical zoom because the overscan is not blanked!
Nr. of steps: 63
Range: 80 .. 120 %

VS: **V**ertical **S**lope Reg: 13 Bit: 5..0 Fu: AL

Adjusts the vertical slope. This alignment is meant to compensate for spread on the value of the external sawtooth capacitor (major) and spread on the internal reference current source (minor). This is the first vertical alignment to execute in order to adjust the internal levels to exact nominal value. These nominal values are important to ensure that all derived correction waveforms (vertical S and horizontal geo) are correct. Use **SBL** (service blanking) for correct alignment. See also chapter geometry alignments.

Nr. of steps: 63
Range: -20 .. +20 %

VSC: **V**ertical **Sc**roll Reg: 18 Bit: 5..0 Fu: UC

Can be used to scroll the picture vertical up and down. Works only when the vertical picture size is zoomed larger than 100 % using **VX**. In this way, the relevant part of the picture can be made visible.
All geometry settings remain correct when scrolling..
It is important to set **VSC** in neutral position before starting alignment!
Neutral position: 1F HEX
Nr. of steps: 63
Range: -18 .. +19 %

VSH: **V**ertical **Sh**ift Reg: 16 Bit 5..0 Fu: AL

Adjusts the vertical shift. This alignment is meant to compensate for vertical offsets like DC offset vertical amplifier (major), mechanical offset picture tube gun (major) and internal offsets (minor). In this way, exact landing in the vertical middle of the screen is ensured when the vertical deflection current outputs are zero. This alignment must be carried out after alignment of **VS** and is important to ensure that all derived correction waveforms (vertical S and horizontal geo) are correct. See also chapter geometry alignments.
Neutral position: $1F_{HEX}$
Nr. of steps: 63
Range: -5 .. +5 %

VWT: **V**ertical **W**ai**T** Reg: 19 Bit: 4..0 Fu: SU

Sets the number of lines to wait before starting the vertical scan. The minimal waiting time is 8 lines, so values smaller than 09_{HEX} have no effect. The working is pending on the various scan modes, see table below.

VGA	VSR	Description	Start of vertical scan
0	X	1 Fh, normal (TV) mode	Fixed
0	0	2 Fh, normal (TV) mode	Falling edge V_D pulse + vertical wait setting
0	1	2 Fh, normal (TV) mode	Rising edge V_D pulse + vertical wait setting
1	X	1 Fh, VGA (multi-sync) mode	Rising edge V_D pulse + vertical wait setting
1	X	2 Fh, VGA (multi-sync) mode	Rising edge V_D pulse + vertical wait setting

Nr. of steps: 23 (09_{HEX} .. $1F_{HEX}$)
Range: 8 .. 31 lines (Setting 00_{HEX} .. 08_{HEX} all give 8 lines delay)

VX: **V**ertical zoom / e**X**pand Reg: 17 Bit: 5..0 Fu: UC

Can be used to shrink the vertical amplitude (compressed 16:9 format on 4:3 tube) or expand the vertical amplitude (4:3 format on 16:9 tube).
The vertical amplitude adjustment is 1 % per step, the neutral position is chosen such (19_{HEX}, 25_{DEC}) that **VX** = 00 gives 25 % picture height reduction (75% picture height), suitable for displaying compressed 16:9 format on 4:3 tube.
When zooming larger than 100 %, vertical overscan larger than 106 % will be blanked to prevent picture tube damage.
It is important to set **VX** in neutral position before starting alignment!
Neutral position: 19 HEX (!!!!!)
Nr. of steps: 63
Range: 75 .. 138 %

2.2.4.5 RGB control and output stages.

Input control bits:

AKB : **A**uto **K**ine **B**iasing Reg: 02 Bit: 4 Fu: SU

With this bit, the automatic black current stabilization loop can be switched off. This can be used for LCD application and is not intended for use with picture tubes. Note that when **AKB**=1, the **WPA** settings do not function.

0 = Automatic black-current stabilisation (ABS) loop enabled
1 = ABS loop disabled (suitable for LCD applications)

BKS : **B**lac**K** **S**tretch Reg: 00 Bit: 2 Fu: UC

This function stretches offsets in black of non standard signals to black level

0 = Black stretch off
1 = Black stretch on (to be switched off for **WPA** adjust)

BLS : **BL**ue **S**tretch Reg: 00 Bit: 3 Fu: SC

This function offsets colours near white to blue above a certain drive level to obtain a brighter white impression.
Note: Blue stretch should be switched off for white adjustment with **WPA**!

0 = Blue stretch off
1 = Blue stretch on

EBB : **E**nable **B**lue **B**ack Reg: 00 Bit: 6 Fu: SC

When no signal is present (SL = 0) a blue screen is inserted.

0 = Blue back off
1 = Blue back on

FBC : **F**ixed **B**eam **C**urrent switch-off Reg: 01 Bit: 6 Fu: SC

When switching to stand-by via I^2C or when the FBSCO (**F**ixed **B**eam **C**urrent **S**witch **O**ff) pin 29 is pulled high (> 2V) the RGB outputs are driven high to deliver a fixed beam current for discharge of the picture tube. The beam current is monitored via the black current loop pin 43.

0 = Fixed beam current switch-off disabled
1 = Fixed beam current switch-off enabled

GAI : **GAI**n of luminance channel Reg: 02 Bit: 5 Fu: SU

Sets the required input level for the Y-input pin 28.

0 = Normal gain (Y input pin 28 black-white = 1 Volt)

1 = High gain (Y input pin 28 black-white = 0.32 Volt)

IE1 : RGB **I**nsertion **E**nable (Fast bl.) Reg: 00 Bit: 1 Fu: SC

When this bit is low, the fast blanking function of pin 33 is disabled, so no external RGB_{IN} insertion is possible.

0 = Fast blanking disabled

1 = Normal fast blanking function

IE2 : RGB **I**nsertion **E**nable (Fast bl.) Reg: 00 Bit: 0 Fu: SC

Enable fast blanking (pin 38) of RGB-2 input. When for RGB-2 the blending function is selected (**OBL** = 1) then **IE2** has no effect, blending is always enabled.

0 = Second fast blanking disabled

1 = Normal fast blanking function

MAT : **MAT**rix selection Reg: 00 Bit: 7 Fu: SC

Selects PAL or NTSC matrix. Standard information should be derived from the used colour decoder.

When RGB1 input is used, PAL matrix should be selected for correct colour reproduction (**MAT** = 0) because the RGB -> YUV conversion is complementary to the PAL matrix.

0 = PAL matrix

1 = NTSC matrix

MUS : **M**atrix **US**A Reg: 01 Bit: 7 Fu: SC

Selects between the two built-in NTSC matrices.

0 = Japanese NTSC matrix

1 = USA NTSC matrix

OBL : **O**SD **Bl**ending Reg: 01 Bit: 5 Fu: SU

Selects blending mode or standard fast blanking for the second RGB input.

With blending, the internal RGB signals can be mixed with the external RGB signals. Changing the voltage level on the BL-2 pin 38 from 0.2 to 1.2 volt reduces gradually the internal RGB from 100 % to 0 % and the external RGB from 0 % to 100 %.

0 = Standard fast blanking

1 = Blending mode selected

RBL : **R**GB **Bl**anking Reg: 00 Bit: 4 Fu: SC

Controls blanking of the RGB outputs. Can be used to keep the picture black at start-up of the set until the CCC loop is stabilised and the cathode emission is high enough to display a decent picture.

Can also be used for blanking RGB outputs when black current loop is disabled (AKB = 1) for LCD applications.

0 = Normal picture visible

1 = RGB_{OUT} (pins 40, 41, 42) blanked

SC1,0 : **S**oft **C**lipping level Reg: 0B Bit: 5,4 Fu: SC

Sets the difference between Peak White Limiting (**PWL**) level and the soft clipping level. Or disables the soft clipping. Using soft clipping prevents overdrive of the RGB output stages (blooming) during e.e subtitles.

SC1	SC0	Voltage difference between Soft Clipping and PWL level
0	0	0 % above PWL level
0	1	5 % above PWL level
1	0	10 % above PWL level
1	1	Soft Clipping off

Output control bits:

BCF : **B**lack **C**urrent loop **F**alse Reg: 01 Bit: 2 Fu: SC

Reflects the condition of the black current loop. Can be used at start-up or for regular check during normal operation to indicate RGB stage malfunctioning.

0 = Black current loop is stabilised
1 = Black current loop is not stabilised

HBC : **H**elp above/below **B**lack **C**urr. loop window Reg: 02 Bit: 0 Fu: AL

Can be used together with **WBC** (**W**indow **B**lack **C**urrent loop) for factory alignment of the Vg2. The bit indicates whether the lowest DC level of the three RGB outputs during cut-off measurement is below or above 2.5 Volts. The lowest RGB output corresponds with the highest cut-off level at the CRT cathode.
Reading HBC indicates which direction to turn the Vg2 potmeter to bring the black current loop in window (see **WBC** below)

0 = below 2.5 Volts
1 = above 2.5 volts

IN1 : RGB **IN**put 1 status Reg: 02 Bit: 2 Fu: SC

Reflects the level on the fast blanking input pin 33.
Level is only checked during vertical retrace to enable differentiation between OSD insertion (**IN1** remains 0) and full RGB sources (**IN1** becomes 1)

0 = Pin 33 low (< 0.3V), no insertion
1 = Pin 33 above insertion level (>0.9V, RGB_{IN} inserted when **IE1**=1)

IN2 : RGB **IN**put 2 status Reg: 01 Bit: 5 Fu: SC

Reflects the level on the fast blanking input pin 38.
Level is only checked during vertical retrace to enable differentiation between OSD insertion (**IN2** remains 0) and full RGB sources (**IN2** becomes 1)
Note that when blending function is selected (**OBL** = 1), **IN2** remains always 0.

0 = Pin 38 low (< 0.3V), no insertion
1 = Pin 38 above insertion level (>0.9V, RGB_{IN} inserted when **IE2**=1)

WBC : **W**indow **B**lack **C**urrent loop Reg: 00 Bit: 0 Fu: AL

Can be used together with **HBC** (**H**elp above/below **B**lack **C**urr. loop window) for factory alignment of Vg2. The bit indicates whether the lowest of the three RGB outputs during cut-off measurement is within a window of 2.4 to 2.6 Volts. The lowest RGB output corresponds with the highest cut-off level at the CRT cathode.
HBC should be used to detect whether the DC level is above or below the window level.

0 = outside window
1 = inside window (2.4 Volt < lowest DC at RGB < 2.6 Volt)

Analogue controls:

BRI: **BRI**ghtness Reg: 5 Bit: 5..0 Fu: UC
Nr. of steps: 63
Range: - 1 .. + 1 V variation with respect to the measuring pulses at RGB_{OUT}

CL3..0 : **C**athode drive **L**evel Reg: 01 Bit: 3..0 Fu: SU
This can be used to adapt the black/white drive of the RGB outputs to match the required drive level for the picture tube. The table gives approximated values.
Nr. of steps: 15
Range: 50 .. 95 Volt drive $_{Black\text{-}White}$

CL3	CL2	CL1	CL0	Variation Cathode Drive Level
0	0	0	0	50 $V_{BL\text{-}WH}$
1	0	0	0	74 $V_{BL\text{-}WH}$
1	1	1	1	95 $V_{BL\text{-}WH}$

CON: **CON**trast Reg: 07 Bit: 5..0 Fu: UC
Nr. of steps: 63
Range: 10 .. 100 % (20 dB)

PWL: **P**eak **W**hite **L**imiting Reg: 0B Bit: 5..0 Fu: SC
Sets the level at which the peak white limiting is activated. The level is related to the 1 Volt pp black to white level of a standard Y input signal
Nr. of steps: 16
Range: 0.55 .. 0.85 Volt black to white at Y input pin 28

SAT: **SAT**uration Reg: 06 Bit: 5..0 Fu: UC
Nr. of steps: 63
Range: 0 .. 300 %

WPR,G,B: **W**hite **P**oint **R**, **G** and **B** Reg: 08, 09, 0A Bit: 5..0 Fu: AL
Adjustment of the white point setting.
Note: When AKB=1 (black current loop disabled), these registers are not functioning
Neutral setting: 1F HEX
Nr. of steps: 63
Range: -50 .. +50 %

2.2.4.6 Power and protection.

Input control bits:

EVG : **E**nable **V**ertical **G**uard Reg: 04 Bit: 1 Fu: SU
With this bit set high, a vertical guard failure will immediately blank RGB_{OUT} to avoid damage to the picture tube. To use this function, a vertical guard pulse has to be connected to pin 9 (Sandcastle / Vertical guard).
When no vertical guard pulse is connected to pin 9, **EVG** must be set to zero to prevent unwanted blanking of RGB_{OUT}.

0 = Only vertical guard detection (output bit **NDF**)
1 = Detection (**NDF**) and protection by blanking RGB_{OUT}

PRD : Overvoltage **PR**otection **D**etection Reg: 03 Bit: 2 Fu: SU
Over-voltage protection input mode: When the bit is high, an over-voltage situation (voltage > 3.9 Volt on pin 50 EHT/XPR) will stop the horizontal drive via slow stop at the first vertical retrace, set the IC in stand-by (**STB1,0** = 0 0) and set bit **XPR = 1**. When the voltage at pin 4 drops again below 3.9 Volt, the IC will remain in stand-by.
When the bit is low, only output bit **XPR** is set to 1 when the voltage on pin 50 exceeds 3.9 Volts.

0 = Only over-voltage detection (output bit **XPR**)
1 = Over-voltage detection (**XPR**) and stop horizontal drive (protection)

STB1,0 : **ST**and **B**y Reg: 02, 03 Bit: 4Fu: SC
When both stand-by bits are set to 1, first calibration takes place and then the horizontal drive is initialised via slow start.
When both stand-by bits are set to 0, the horizontal drive is stopped via slow stop and the RGB outputs are blanked or set for 1 mA discharge, pending on **FBC**.
Note that **both** bits have to be toggled before is switched from stand-by to operational and vice versa. Toggling only one **STB** bit has no effect! In this way, the behaviour is more robust against distortion on the I^2C lines.
See I^2C start-up procedure for the correct start-up procedure before setting **STB1,0** to 1 1.

STB 1	STB 0	Function
0	0	Stand-by
0	1	Keep last status
1	0	Keep last status
1	1	Operational

Output control bits:

NDF : **N**o vertical **D**e**F**lection Reg: 01 Bit: 3 Fu: SC
This bit is set to 1 when the vertical guard pulse at pin 9 (Sandcastle / Vertical guard) is wrong.
0 = Vertical deflection OK (correct guard pulse present)
1 = Failure detected in the vertical output stage (incorrect guard pulse present)

POR : **P**ower **O**n **R**eset Reg: 00 Bit: 7 Fu: SC
Power on reset: Indicates detection of a power failure (including power down during stand-by or switch-off of the TV set). It remains high until the status bytes have been read successfully to enable also to detect short power failures. When a failure is detected, the internal data is not reliable any more and should be refreshed. During normal operation the POR status should be read continuously, before sending any input data. During start-up, the IC status should be read until the POR bit is low, immediately followed by the start-up procedure (see chapter 2.2.4 .)
0 = Device operational
1 = Power failure detected

XPR : **X**-ray **PR**otection Reg: 00 Bit: 4 Fu: SC
This bit is set to 1 when an overvoltage is detected (voltage on pin 4 EHT / XPR > 3.9 Volt) See also **PRD** (reg. 0B, bit 6 I/O = I)
The bit is latched when the voltage on pin 4 > 3.9 Volt and can only be set to zero when the status bytes are read after the voltage on pin 4 has dropped below 3.9 Volt. The µprocessor can check reading XPR when the IC is set in stand-by mode (if enabled by **PRD**=1)
0 = No over-voltage detected
1 = Over-voltage detected on EHT input pin 4

2.2.4.7 Device select.

Output control bit:

ID2..ID0: Device **ID**entification code Reg: 01 Bit: 7..4 Fu: SC
This can be used to find out which IC type is connected.
This makes it possible to let a software control system configure itself to the available functions, e.g. for VGA or non-VGA

ID3	ID2	ID1	ID0	Type number	Functions
0	0	0	0	TDA9330H	No VGA, DAC output I^2C controlled
0	0	0	1	TDA9331H	VGA, DAC output proportional to VGA horizontal frequency
0	0	1	1	TDA9332H	VGA, DAC output I^2C controlled

3. APPLICATION INFORMATION

3.1 General

In section 2 device information has been given. This section describes the application aspects of the pins.
The component choice often is a compromise and depends on the requirements defined by the customer.
By means of this section one is able to decide whether components can be changed and what the consequences will be.
Please refer to C 1 for a complete application diagram of the TDA933X.

3.2 Application remarks per functional block and per pin

The pins will be described per functional block analogue to section 2. The pin voltage may not exceed ground - 0.5 V or Vcc + 0.5 V.

3.2.1 Horizontal synchronisation

*** Flash detection input** **pin 5**

This input can be used to switch-off immediately the horizontal output. The pin should be pulled high by an external flash detection circuit.
The detection level for switch-off is 2 Volt. For noise immunity, the input has a hysteresis of 0.2 Volt.
When the voltage at the input drops again below the detection level, the horizontal output is switched on again via the slow start procedure.
The function of this input is hard wired and is meant for severe disturbances which need direct action like flash-over when I^2C control also might be not reliable.
Because short spikes (10 ns) can trigger the input, a flash detection circuit should be connected to pin 5 via a low pass RC filter with the capacitor placed direct on the pin with short connection to ground.
The status of pin 5 can be read out via the bit **FLS**. When the input level of pin 5 is above detection level, **FLS** is set to 1, when the level drops below detection level **FLS** becomes 0 again..
For another protection option, see overvoltage protection on pin 4, chapter vertical synchronisation, vertical drive and geometry corrections below.

*** Horizontal drive,** **pin 8**

This open collector output is meant to drive the horizontal output stage. The output is active low, i.e. the line output transistor should conduct during the low period of the output.
The different conditions of the horizontal drive output are:

- slow start:
  - after power-on and all registers are loaded
  - when switching-on from stand by using **STB1,0**
  - after release of flash protection on pin 5 (Flash input, voltage < 2 Volt)
- running
  - Normal condition, 48.2% off / 51.8% on duty cycle (48.2% high, 51.8% low)
- slow stop:
  - when switching-off to stand by using **STB1,0**
  - after activation overvoltage protection **XPR** (pin 4, voltage > 3.9 Volt) when enabled (**PRD**=1)
- disabled (direct stop)
  - when the voltage drops at supply pins 17 and 39 below **POR** level (see section supply)
  - when flash protection is activated by forcing pin 5 (Flash input) high (voltage > 2 Volt)

For optimal sync stability it is recommended to have the output current as small as possible. This can be achieved by a small series resistor (100Ω) direct after the pin and a low output amplitude <5V. An extra emitter follower on the output can also be used.

*** Sandcastle output/Vertical guard input pin 9**

The sandcastle output is synchronised with the display drive and can be used to synchronise external display devices like TXT or PIP.
The level during scan is ≤ 0.5 Volt, during horizontal and vertical blanking 2.5 Volt and during clamp pulse 4.5 Volts. The clamp pulse and vertical blanking are always present.
The start of the horizontal blanking is related to the internal horizontal timing and starts after 91% of the line time is expired, referred to the middle of the last horizontal flyback pulse. This ensures that the horizontal blanking always starts early enough to avoid foldover of the picture. The vertical blanking ends when the trailing edge of the flyback pulse on pin 13 drops below 0.3 Volt.
The clamping pulse timing is the same as the clamping pulse used for the Y and RGB input signals.
The output is a push-pull configuration with a typical source/sink current of 0.7 mA. Because of this limited drive current, when a long track is connected to this pin, parasitic capacitance can deteriorate the edges. In this case, a buffer should be applied.

The sandcastle output is combined with the vertical guard input. With this input the correct working of the vertical deflection circuit can be monitored.
The status of the vertical guard input is reflected in output bit **NDF**.
During each vertical blanking period a current between 1 and 3 mA should be injected to pin 9 during at least 1 line to keep **NDF** = 0 indicating correct working of the vertical deflection.
When no current or a too low current is injected during vertical blanking or when a continuous current above 1 mA is injected, **NDF** is set to 1, indicating a vertical deflection failure.
The bit **NDF** can be read out by the µprocessor. When also **EVG** is set to 1, the RGB outputs are blanked when **NDF**=1 to protect the picture tube against burning-in when no vertical deflection is present.
Note that when the vertical phase changes, e.g. after a channel change, it is possible that **NDF** is set to 1 for some fields before the new vertical pulse V_D is catched. We advice therefore to monitor a few fields **NDF** before taking decisions like shut down of the TV set to prevent overprotection in normal situations.
The vertical deflection family TDA835X has a suitable vertical guard output, which can be connected via a series resistor of 100 Ohms direct to pin 9, see Fig 13 below. When the sandcastle is needed by other applications before the supply voltage of the vertical deflection is present, an extra diode must be inserted, anode to the vertical guard output pin, cathode to the 100 Ohms resistor. In this way, pulling down of the sandcastle output by the internal protection diodes of the vertical deflection IC is prevented.

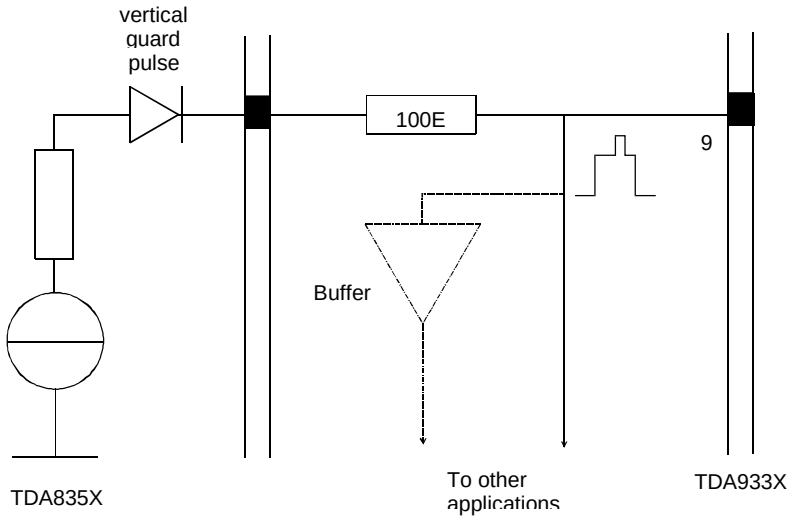


Fig 13 : Interface vertical guard pulse

*** Horizontal frequency selection pin 12**

For robustness, the selection between 1 Fh mode and 2 Fh mode is hard wired via this pin.
For 1 Fh mode, it must be connected to ground. For 2 Fh mode, the pin must be left open.
If for an application switching between 1 Fh and 2 Fh mode is needed, this can be achieved by connecting a switch transistor between pin 12 and ground. The level at pin 12 is only checked when starting up from stand-by, i.e. when **STB1,0** are toggled from 0 0 to 1 1. Changing the level at pin 12 in operational mode when H-out is running will not change the H-out frequency until the TDA933X has been set to stand-by (**STB1,0** = 0 0) and switched on again (**STB1,0** = 0 0). However, for safe operation under various conditions (e.g. power dips) we advice **to switch pin 12 only when the TDA933X is in stand-by mode!**
For extra protection, the status of pin 12 is latched internally when the IC is switched on from stand-by mode (setting **STB1,0** from 0 0 to 1 1). In this way, spikes or disturbances during normal operation will not disturb the horizontal drive.
For all the various frequencies in TV mode and VGA mode for 1 Fh and 2 Fh, see the device description and/or H_D input pin 24 below.

*** Flyback input pin 13**

The line flyback pulse, fed to this pin, is used for two functions:
- input signal for the PHI-2 loop and
- RGB line blanking. (without flyback pulse blanking occurs only during the clamping pulse)

The slicing level for the PHI-2 loop reference is chosen at 4.0 Volts. The flyback pulse generation should be designed to give optimum stability on this level. Please note that the flyback pulse width may not vary on beam current variations because they can not be compensated by the PHI-2 loop.

The RGB line blanking starts when the flyback pulse on the input rises above 0.3 Volt. This low level makes it easy to obtain a sufficient wide horizontal blanking which starts in time.

In Fig 14 an application proposal is given for the flyback pulse.

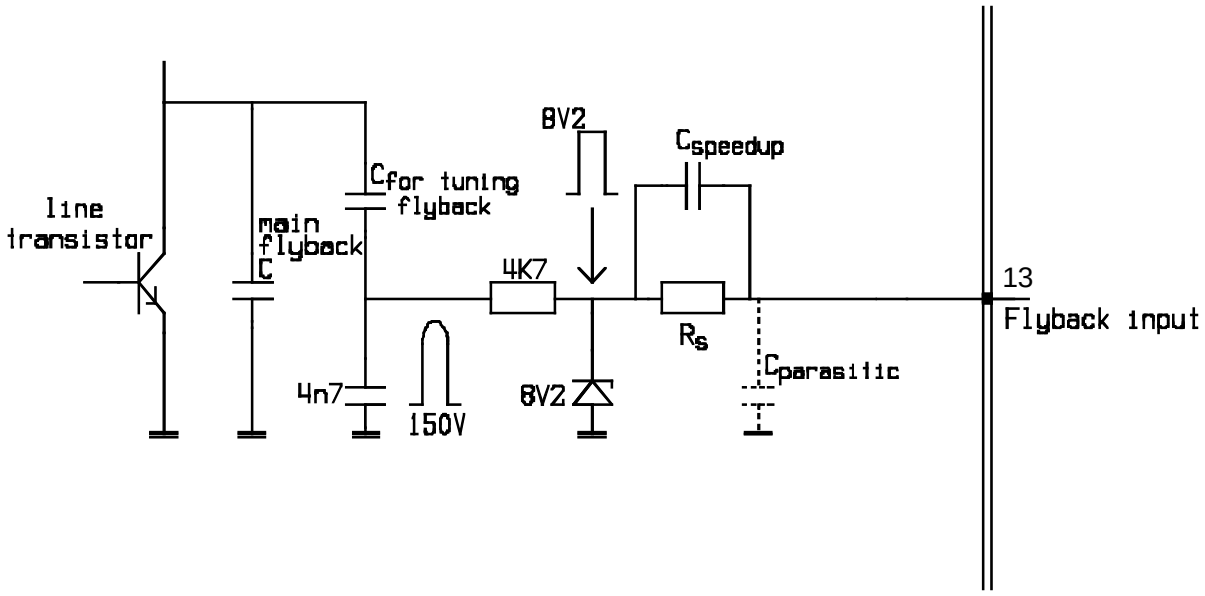


Fig 14 : Flyback input circuit

A capacitive divider in parallel to the line transistor is used to derive a flyback pulse with a height of about 150 Volts peak. In this way we ensure steep edges for optimal jitter performance and optimal blanking width for the RGB outputs.
This pulse is limited to 8.2 Volts (V_{peak}) via a resistor of 4.7 kΩ and a zener. In the layout, care should be taken that the 30 mA peak current through the zener does not disturb the IC application.
The series resistance is to protect against flash and should be chosen such, that the edges are still steep enough at pin 13 to ensure proper RGB blanking and PHI-2 jitter. Usual, 1 - 4.7 kOhm will be ok. If needed, the edge steepness can be improved by placing a small speed-up capacitor in parallel to R_{series} to compensate for parasitic capacitance.

The presence of a flyback pulse can be read out via **NHF**. Using **NHF** the µprocessor can check whether the horizontal deflection circuit is working.

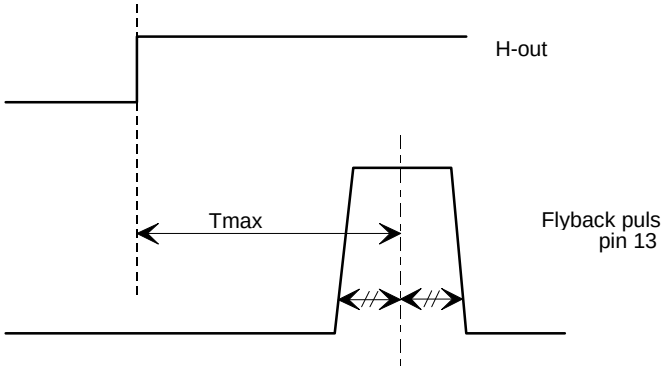
*** PHI-2 dynamic phase compensation input pin 14**

Besides the phase dynamic phase compensation, also some other important parameters of the PHI-2 loop for application are summarised below.

PHI-2 Loopfilter:
The loopfilter is a first order filter. The filter is built-in. The correction factor K is 0.5, which means that a phase error between PHI-2 internal reference and flybackpulse is halved each line period.

PHI-2 Loopgain:
The static loopgain (K) is minimal 500µs/µs. This implies that phase variations (δt_0) due to storage time variations (δt_d) are reduced by this factor of 500.

Shift control range:
The picture can be centred on screen by means of the horizontal shift (**HS**) via I²C bus. The range is +/- 4.5 µs for 1 Fh and +/- 2.25 µs for 2 Fh.
The delay between the positive going Hout (line transistor switches off then) and the centre of the flyback pulse (ref PHI-2) is pending on the line frequency and may range from 0% to 37% of one line period. So for 1 Fh the delay must be ≤23.6 µs and for 2 Fh ≤ 11.8 µs. See Fig 15.



Tmax ≤ 37% x Tline
≤ 23,6 µs (1Fh)
≤ 11,8 µ (2Fh)

Fig 15 : PHI-2 timing signal

The horizontal shift range is chosen large enough to compensate for centring errors with a variety of picture tubes. Under normal conditions it is therefore possible, that active video can be shifted in the retrace period, leading to a folded picture at the side. (see Fig 16)

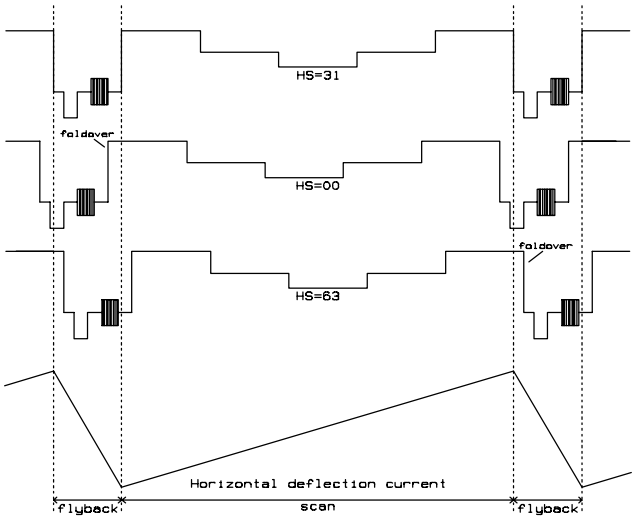


Fig 16 : Horizontal shift.

Parallelogram correction
The angle of the vertical lines can be adjusted by means of **PC** (**P**arallelogram **C**orrection). Via this register it is possible to add a fixed horizontal shift per line in the PHI-2 loop from top to bottom.
The correction range is (horizontal shift measured from the vertical centre of the screen to the top or bottom):

For 1 Fh: +/- 0.54 µs
For 2 Fh: +/- 0.27 µs

Parallelogram correction helps to set the vertical lines orthogonal on the horizontal lines when the horizontal and vertical deflection yokes are not orthogonal.

Dynamic phase compensation via pin 14:
The flyback pulse width may not vary on beam current variations because they can not be compensated by the PHI-2 loop. The phase shift error on screen will be half the flyback pulse width variation.
If this demand can not be reached in the line output stage an external compensation circuit might help to overcome such phase variations. A voltage, related to the EHT voltage, can be fed back to pin 14.
The voltage on this pin is 4.0 Volts for no compensation. The control sensitivity for dynamic phase compensation is:

For 1 Fh: 0.4 µs / Volt
For 2 Fh: 0.2 µs / Volt

The input voltage range is 1.5 to 6.5 Volts.

Internal, pin 14 is connected to an internal reference voltage of 4.0 Volt via a resistor of 100 kOhm. The input impedance is therefore also 100 kOhm.

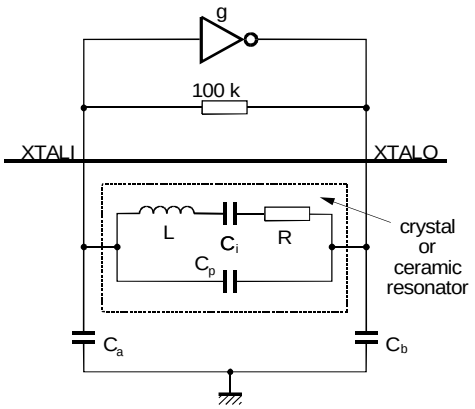
The polarity of the input is chosen such, that normal used circuits to measure the EHT voltage decrease for the beamcurrent limiting function can directly be used. In other words, the EHT info voltage should drop when the EHT voltage drops.

When the pin is not used, it should be decoupled with a capacitor of 100 nF to ground.

*** Reference oscillator** **pin 20, 21**

The reference oscillator uses an external resonator or X-tal of 12 MHz. The choice for resonator or X-tal depends on the required accuracy of the free running frequencies. Deviations of the reference frequency are added to the deviations as specified for the horizontal end vertical circuits. In practice, resonators are accurate enough for standard TV applications.

In the figure below, the design criteria are given for the oscillator circuit:



$$f_{osc} = \frac{1}{2\pi \cdot \sqrt{L_i \cdot \frac{C_i \cdot C_{load}}{C_i + C_{load}}}}$$

$$C_{load} = C_p + \frac{C_a \cdot C_b}{C_a + C_b}$$

requirement for start-up:

$$C_{load}^2 \cdot R_i \leq 1.1 \cdot 10^5$$ (Ri in Ohm) (Cload in pF)

Fig 17 : Simplified diagram X-tal oscillator

The transconductance g_m = 5 mA/V (4 mA/V minimal), the maximum allowed series resistance of the resonator = 30 Ohms for 30 pF load capacitance (standard value for resonators, because X-tals usually have a lower load capacitance a higher series resistance is allowed) .

Both capacitors C_A and C_B should be connected as short as possible to ground pin 19 for optimal stability. Keep the loops and connections in the oscillator circuit as small and short as possible.

For EMC, the oscillator amplitude is kept below 1 Volt pk-pk.

It is also possible to use an external reference signal of 12 MHz. The amplitude should be between 2 and 5 Volt pk-pk and the signal should be fed to pin 20.

The locking of the horizontal VCO to the reference oscillator can be read out via bit **NRF**. When **NRF** = 1, the horizontal VCO is not locked and the horizontal output can not be enabled because the horizontal frequency is not known then.

*** Low power start-up pin 22**

To start-up the H-out, only 5 volt has to be supplied to this pin while no 8 Volt is present on pin 17 and 39. The 5 Volt can be often derived from the stand-by voltage for the microprocessor. The typical current consumption is only 3 mA.
An application example is given below.

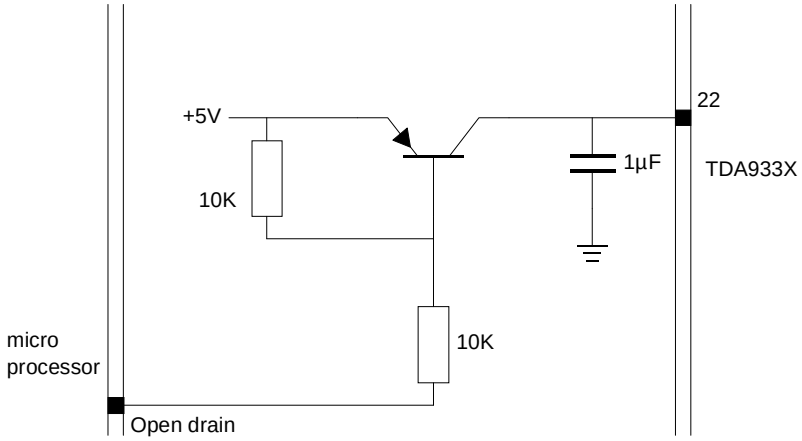


Fig 18 : Low power start-up circuit

The procedure is as follows:

- Microprocessor switches on + 5 Volt. The H-out will start with a fixed off time of 48.2 % while the on time increases from 0 to 12.5 % (all percentages refer to the final cycle time of H-out). The load of the horizontal drive can be used to wake up the power supply from stand-by mode. It is also possible to supply the 8 Volt to pin 17 and 39 using scan rectification of the FBT.
- Check till **POR** = 0 (+8 Volt is present)
- Write all I^2C registers with **STB1,0** = 0 0.
  Note that after reading POR = 0 all I^2C registers should be written within two fields time. Else the H-out is switched-off via a slow stop because malfunctioning is assumed.
- Check till **NRF** = 0 (horizontal oscillator locked to reference oscillator)
- Set **STB1,0** = 1 1. The slow start of the H-out will be completed.
- Switch off the +5 Volt supply from pin 22. When the 5 Volt remains present, the horizontal output cannot be switched off completely and will remain running on 12.5% on / 48.2 % off when the TDA933X is set in stand-by. This problem can happen when the TDA933X is switched off by **STB1,0** = 0 0, or when **POR** = 1 after a power dip or when **XPR** = 1 and the TDA933X is set to stand-by via slow stop (when enabled via **PRD** = 1).

Using the low power start-up can simplify the power supply design of the set.

*** H_D input pin 24**

Because the acquisition loop PLL is completely integrated, also the most important parameters of this loop will be covered here.

The H_D input is compatible with standard digital levels:

Low voltage: < 0.8 Volt
High voltage: > 2.0 Volt

For optimal jitter performance, a Schmitt trigger input is used. The input is high ohmic.
The rise and fall time of the edges from the H_D pulse should be ≤ 100 ns, the minimal pulse width is 1 µs.

Acquisition loop
The PLL loop filter is built-in. The loop speed can be increased by 30% when setting bit **FAST** to 1.

The holding / catching range and the free running frequency of the acquisition PLL is:

TV mode:
1 Fh: 14.9 - 17.15 kHz, free running frequency (when not locked): 16.05 kHz
2 Fh: 29.8 - 34.3 kHz, free running frequency (when not locked): 32.1 kHz
Note that the catching range and the free running frequency is chosen such, that for 2 Fh as well standard transmissions as horizontal frequencies of 33.75 kHz for MUSE (Japanese analogue HDTV) and digital HDTV, defined within the ATSC standard (USA) can be handled.

VGA mode:
1 Fh: 15 - 25 kHz, free running frequency when not locked: 16.05 kHz
2 Fh: 30 - 50 kHz, free running frequency when not locked: 32.1 kHz

The deviation of the free running frequency is +/- 1%. The deviation of the reference oscillator should be added to obtain the final deviation.

Note: 1 Fh and 2 Fh mode can be selected by connecting pin 12 (horizontal frequency select input) to ground (1 Fh) or leaving the pin open (2 Fh). See above.

To prevent damage to the horizontal deflection stage, the correction speed of the acquisition loop is limited:

TV mode:
1 Fh: +/- 2 µs / horizontal line
2 Fh: +/- 1 µs / horizontal line

VGA mode:
1 Fh and 2 Fh: 100 kHz / s

When the acquisition loop is locked to an incoming H_D pulse, **SL** = 1 This bit can be used to detect a valid incoming H_D pulse.

The acquisition loop can be forced in free running mode by setting **POC** = 1. For the horizontal frequency, see the free running frequency above. The vertical free running frequency is set by **SVF** and **VFF**.
When **POC** = 1, **SL** is always 0 so no detection of a valid H_D pulse is possible. To detect valid input signals, an external coincidence circuit must be used, e.g. from the input processor TDA9321.

*** DAC output pin 25**

This DAC output has a range from 0.3 to 4.0 Volt (typical). The output impedance depends on the output voltage and ranges from 10 kOhm for 0.3 Volt to 300 Ohm for 4.0 Volt. The output configuration consists of a NPN emitter follower with an internal resistor of 50 kOhm to ground.
The function of this output is pending on the IC version.

For TDA9330 and TDA9332, the DAC output voltage can be lineary set in 63 steps via I^2C from 0.3 to 4.0 Volt.

For TDA9331, the DAC output voltage changes in VGA mode proportional with the centre frequency of the line oscillator. For the lowest centre frequency (16/32 kHz 1Fh/2Fh) the output voltage is 0.3 Volt, for the highest centre frequency (24/48 kHz 1Fh/2Fh) the output voltage is 4.0 Volt. This voltage can be used to adapt the supply voltage for the horizontal deflection when the horizontal frequency changes.
In TV mode, the output voltage of pin 25 is minimum, so 0.3 Volt.

3.2.2 Geometry (drive of vertical deflection) and Vertical & Horizontal

*** Vertical drive** **pin 1,2**

The vertical drive has a current output. The output is balanced which ensures a good common mode behaviour with temperature and makes the output signal less sensitive for disturbances.
The figure below gives the vertical drive signals with the vertical output stage TDA8350.

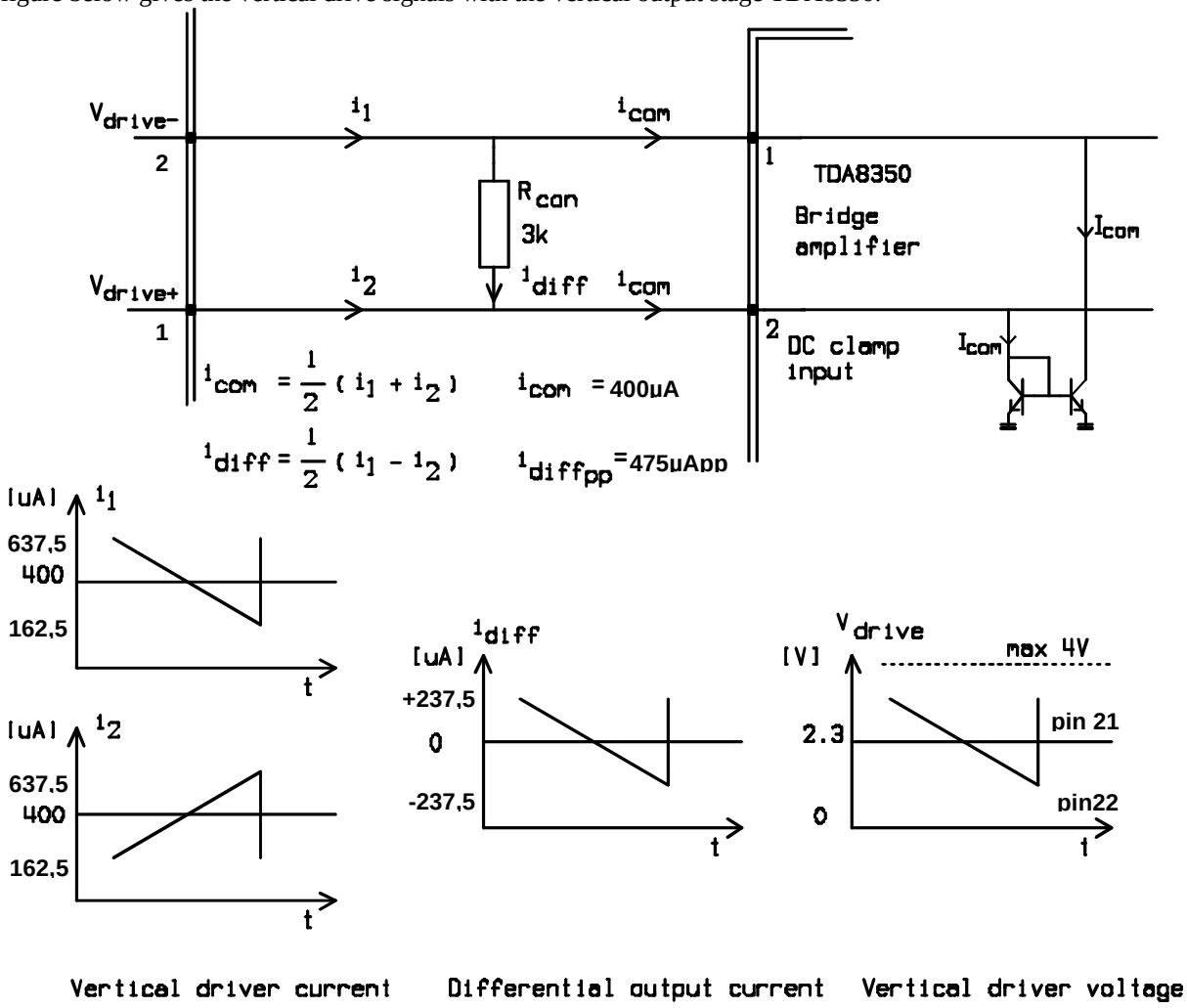


Fig 19 : Vertical drive signals with TDA8350

The differential output voltage is determined by the conversion resistor Rcon and the differential output current.

$$U_{diff} = i_{diff\ pp} * Rcon = 475\ \mu A_{pp} * 3k\Omega = 1.425V_{pp}$$

Important for the TDA933X is that the voltage at the driver pins does not exceed 4V.
The value for Rcon=3kΩ is determined by the TDA8350.
Rcon must be connected closely to pin 1 and 2 of the TDA8350 for optimal EMC behaviour.
The DC voltage at pin 46 is determined by the DC clamp input of the TDA8350.

*** EW drive, pin 3**

The EW drive is a current output. The output is single-ended and is fed directly to the EW-input pin 12 of the TDA8350. Figure below gives the EW output configuration.

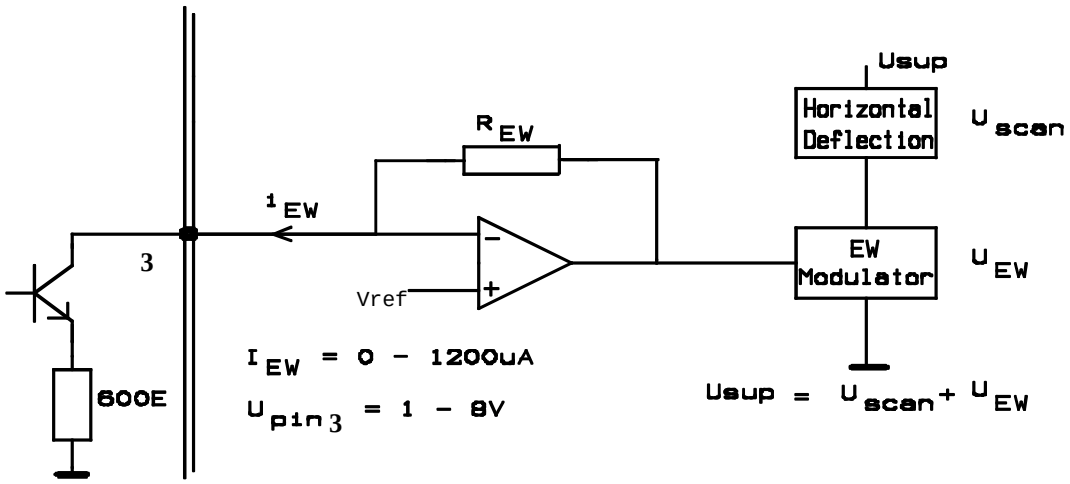


Fig 20 : EW output configuration

The DC voltage on pin 3 is determined by the East-West driver stage input and may range from 1 to 8 Volts.
To prevent distortion, the voltage must always be > 1 Volt.
The DC voltage on pin 3 is equal to the voltage Vref (see Fig 20). Because this DC voltage on pin 3 is equal to the minimal output voltage of the East-West driver stage (reached for $i_{ew} = 0$), it is recommended to choose Vref close to 1 Volt for maximum range.

For the TDA 8350, this voltage level on the input is determined by the "EW reference" pin 13, which sets Vref internally.

It is recommended to minimise the EW-output current by means of the EW-width setting.
A minimum EW-current implies a minimum EW-voltage in the line deflection, Uew.
Doing so results in a minimum power supply voltage; Ub= Uscan + Uew

The minimum EW-current is 0mA and can not be negative. This implies that for the EW-current a margin has to be taken into account for negative current corrections as EHT tracking and trapezium. This margin can be made with the EW-width setting.

Note that for 16:9 displays another optimum is necessary to enable zoom functionality.

For a correct EHT tracking (compensation of picture height and width for variation of the EHT voltage due to beam current loading), the tracking must be the same on vertical and EW. The tracking on vertical is +/-5% (internally fixed). The tracking sensitivity on EW can be set by I^2C register **HCS** in 63 steps from 0 to +/-7% to match the vertical sensitivity.

*** EHT tracking/ overvoltage protection, pin 4**

The input range for EHT tracking is 1.2 - 2.8V, for a compensation of +/-5% on vertical (internally fixed).
The tracking on EW can be set between 0 and +/-7% by **HCS**, to match the vertical sensitivity, see above.
The nominal voltage of pin 4 for no compensation is 2V.

The EHT feedback signal must be filtered in order to prevent disturbances in vertical and/or EW deflection. A compromise has to be determined for tracking speed on normal EHT variation and ripple immunity.
The tracking should be designed for correct vertical compensation, because the vertical sensitivity is fixed internally.

The overvoltage protection is activated when the voltage on pin 4 exceeds 3.9V typical. The result is:
- **XPR** is set to 1 and can be read by the µprocessor
- If **PRD** was set to 1, the horizontal output is disabled after slow stop and the IC is set in stand-by (**STB1,0** = 0 0).

If the overvoltage protection is not used, it is recommended to set **PRD** to 0.

*** Vertical sawtooth, pin 15**

This pin requires a capacitor to ground of 100nF +/- 5%. Short connection to the ground pin 19 of the TDA933X is required.

Important: For this capacitor, a type with good temperature behaviour, long term stability and low leakage must be chosen. Change of the capacitance value due to temperature and/or ageing leads to a proportional change in vertical amplitude. Tolerance of the external capacitor can be compensated by means of the vertical slope adjustment of I²C bus function **VS**. The charge current can be fine tuned with +/- 20%.

The optimal sawtooth amplitude is 3.0 V and is determined by the external capacitor and charge current. For R = 39kΩ at pin 52, the vertical slope **VS** = 1F and field frequency = 50Hz, the charge current is 16 µA. For 60Hz the charge current is increased by 19%. For 100/120 Hz the charge currents are doubled. The sawtooth bottom-level is 2.3V.

In VGA mode, the charge current is adapted to generate a sawtooth with an amplitude of 3.0 Volt pk-pk, independent of the vertical frequency.

The vertical retrace time is determined by the discharge current of 1.2 mA and lasts minimal 7 horizontal lines.

Spurious signals on the sawtooth:
Because the sawtooth signal at this pin represents the deflection current, every disturbance influences the deflection.
Notice that $3.0V_{pp}$ ramp amplitude corresponds to approx. 300 lines. Thus δV_{ramp}=10mV/line in one field.
Due to interlacing this figure becomes 5mV/line over 2 fields. Or, 1mV disturbance on the sawtooth means 1/5 = 20% interlace error.
Thus, for proper interlacing special attention is required on grounding from components, related to the vertical sawtooth and the connection to the inputs from the vertical deflection driver.

*** Reference current, pin 16**

This pin requires a resistor to ground. The optimal reference current is 100µA which is determined by this resistor. The voltage on this pin is 3.9 Volts, which leads to the recommended resistor value of 3.9V / 100µA = 39kΩ +/- 2%
A short connection of this resistor to the ground pin 19 of the IC is recommended for EMC behaviour.

This 100µA reference current should not be changed because the geometry processor is optimised for this current. Furthermore the output current of vertical drive and EW are proportional to this current.

Also for this component a type with good temperature behaviour and long term stability must be chosen. Value changes lead to proportional changes of vertical amplitude and all E/W correction signals.

*** V_D input pin 23**

The V_D input is compatible with standard digital levels:

Low voltage: < 0.8 Volt
High voltage: > 2.0 Volt

The rise and fall time of the edges from the V_D pulse should be ≤ 100 ns, the minimal pulse width is 1 line.

The edges of V_D should preferably be positioned on ¼ and ¾ of the line, referred to the rising edge of the H_D signal. This is related to the internal sampling clock for determination of the odd/even field condition, see device description.

The rising edge of the V_D pulse initiates the reset of the vertical counter on the next internal sampling clock.

The start of the vertical scan can be set in 2 Fh TV mode and VGA mode (1 Fh and 2 Fh) by **VWT**. The number of lines before start of vertical scan can be set between 8 and 31, counted from the rising edge of V_D.

Only in 2 Fh TV mode, the trailing edge of V_D can be set as reference for the number of lines, counted before start of vertical scan by setting **VSR** = 0. In this setting, also the determination of the odd/even field is related to the trailing edge instead of the rising edge of V_D. The **VSR** bit has no influence on other modes.

Alignment of the vertical end EW.
See the section about Geometry Alignment.

*** Zoom function, I^2C: EW, VS, VSC, VX**

Special linear zoom facilities on both Vertical and East-West gives the possibility to adapt the picture size for both 16:9 and 4:3 screens, see Fig 21. When zoom is used, the geometry correction remains correct in both vertical and horizontal direction. Using **VSC** (Vertical Scroll) the (expanded) picture can be shifted up and down. By programming the vertical slope, **VS**, subtitles at the bottom part of the picture can be made visible while the picture position at the top of the screen remains fixed (subtitle mode).

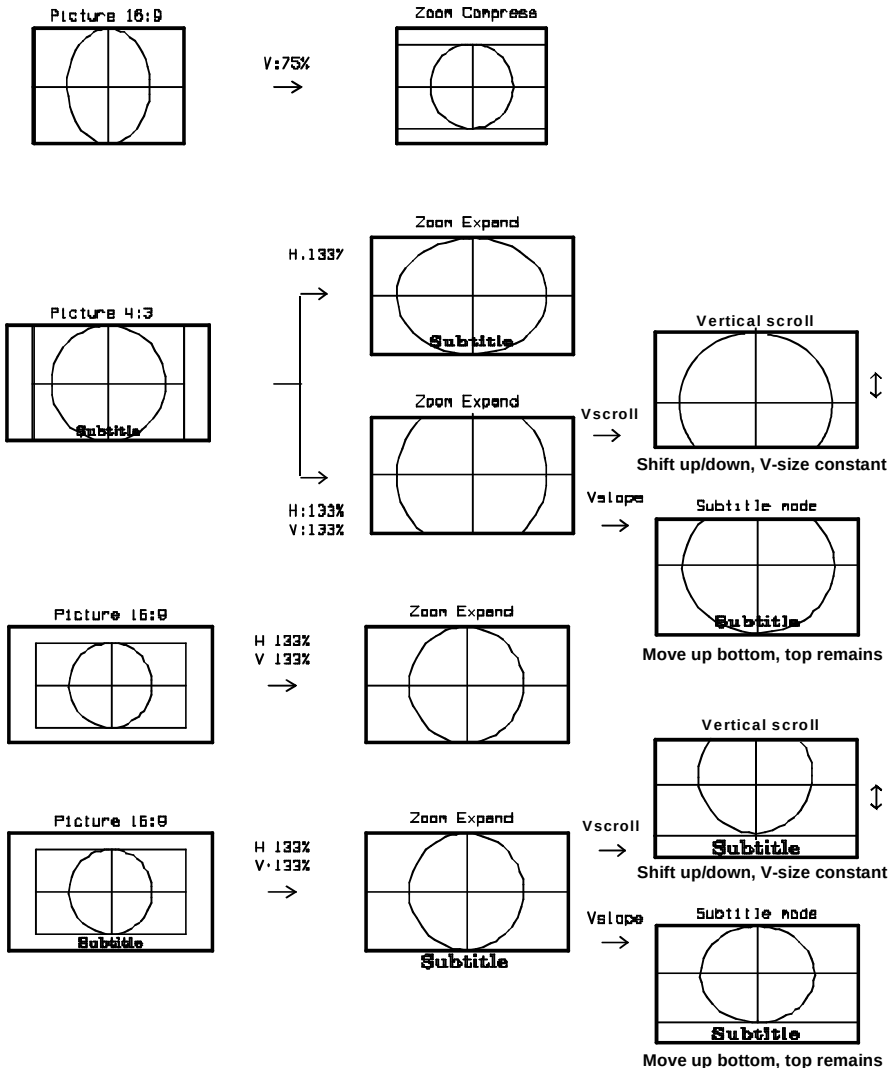


Fig 21 : Expand and compress mode behaviour

Scale factor for H or V	Vert. adjust with **VX** (1% /step)	Hor. adjust with **EW** (0.55% / step)
133% (≡4/3)	58	preset + 18
100% (≡1)	25	preset
75% (≡3/4)	0	preset - 14

Table 5 : H/V settings for aspect ratio's as 16:9 and 4:3

3.2.3 RGB processing and control.

REFER ALSO TO RELEVANT I²C BUS FUNCTIONS.

*** Y,U and V inputs pin 26, 27, 28**

The nominal YUV input signals MUST be AC coupled to inputs pin 28, 27 and 26. Coupling capacitors of 100nF should be used. These signals are internally clamped. The clamping action is slow to ensure optimal clamping performance for noisy YUV signals.
In case a scan conversion box or feature IC's are placed in front of the YUV input be sure that the maximum peak to peak video amplitude does not exceed 2V.
The Y_{IN} signal can be amplified, approximately 10dB, by means of the I^2C bit GAI.
Because of the high input impedance outside burstkey clamping, it is advised to minimise the track length to this luminance input pin. Adequate ground shielding of the luminance signal track is advised for good interference immunity.

*** R_{IN}, G_{IN}, B_{IN} inputs pins 30, 31, 32**

The R_{IN}, G_{IN}, B_{IN} input signals (nominal signal amplitude of 700mV) are AC coupled to pin 30, 31 and 32 respectively. Clamping action occurs during burstkey period. The coupling capacitors chosen are a compromise between fast clamping action and minimum line sag. Capacitors of 22nF or larger can be used .
Source impedance of the R_{IN}, G_{IN}, B_{IN} signals should be minimised for correct clamping operation.

*** RGB 1 insertion switch input pin 33**

In the table below a survey is given of the three modes which can be selected with a voltage on RGB insertion switch input pin and I^2C bit IE1:

V pin 33	I²C function	selected RGB signals:
0.45V<Vpin 33	IE1 = *	RGB (internal)
0.9V <Vpin33< 3V	IE1 = 0	RGB (internal)
0.9V <Vpin33<3V	IE1 = 1	R_{IN};G_{IN};B_{IN} (fast insertion on pin30,31 en 32)

RGB internal is always selected whenever the voltage at pin 33 is lower than 0.45V and is independent on the status of the I^2C control bit **IE1**.
With the I^2C control bit **IN1** it is possible to sense the voltage on the RGB insertion switch input pin 33 continuously even if the I^2C bit **IE1** is disabled. The status of pin 33 is only checked during vertical scan. In this way only full RGB insertion (pin 33 continuous above 0.45 Volt) is indicated, not OSD insertion via e.g. descramblers.
At the input pin of the RGB insertion switch a low (source) impedance (< 560Ω) should be connected for driving this pin.

*** R_{IN2} ,G_{IN2}, $B_{IN\,2}$ inputs pins 35, 36, 37**

See information given at R_{IN1},G_{IN1},B_{IN1} inputs

*** RGB 2 insertion switch input pin 38**

In case the blender function is inactive (OBL=0) this pin 38 behaves in the same way as pin 33 RGB1 insertion switch input. Except now: RGB internal is always selected whenever the voltage at pin 38 is lower than 0.3V
If the OBL-bit is set by I^2C then the RGB 2 insertion switch input acts as an analogue input. The applied voltage represents the amount of blending between the selected internal video-signals and the RGB2 -signals. In graph below the relation between input signal and the blending amount is given. The blending function is optimised for the blender output of the SAA5800 (Artist IC) This device is a combined microcontroller / teletext decoder.

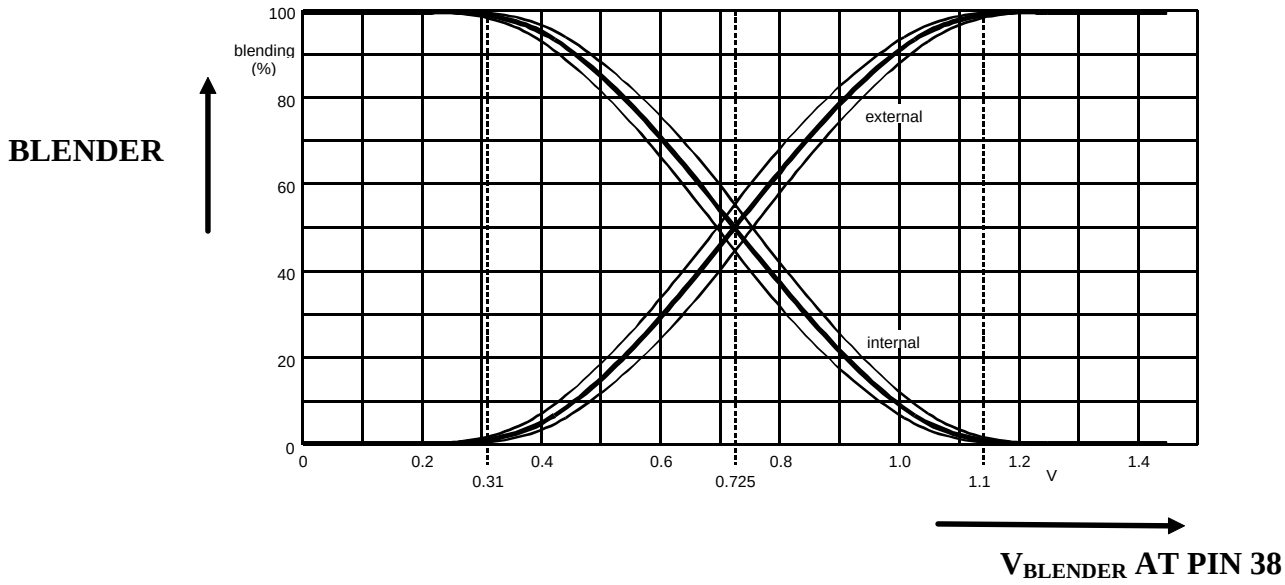


Fig 22 : Blender Output

***PWL capacitor pin 34**

At pin 34 a capacitor of 10pF is recommended for good Peak White Limiting action. Other capacitor values are allowed. If a large capacitor is used the PWL-function starts to react on larger video content signals. (lower frequency video content). The amount of peak white limiting is controlled by 4 bits I^2C register **PWL** (**P**eak **W**hite **L**imiting).
The PWL-capacitor should be placed as close as to pin 34 and the GND of the IC in order to avoid disturbance from external signal sources on the peak white limiting function.

*** Beam current limiting input pin 43**

The average beam current should be measured externally via a low pass filter R_2C_2. . The capacitor value of C_2 can be quite large (10µF).The maximum beam current is determined by the pull-up resistor R_1 and the supply voltage (+V). The time constant R_1C_1 should match the time constant of the internal impedance of the EHT generator (FBT) with the picture tube capacitance
Because the internal peak white limiting function reduces the contrast by pulling internally pin 43 low with a small current source, a diode should be placed in series with pin 43 to enable fast pull-down of pin 43 by the PWL function.
By omitting the diode, the PWL function will be inactive because the small current source cannot discharge C_2 fast enough.
A standard application is given below.

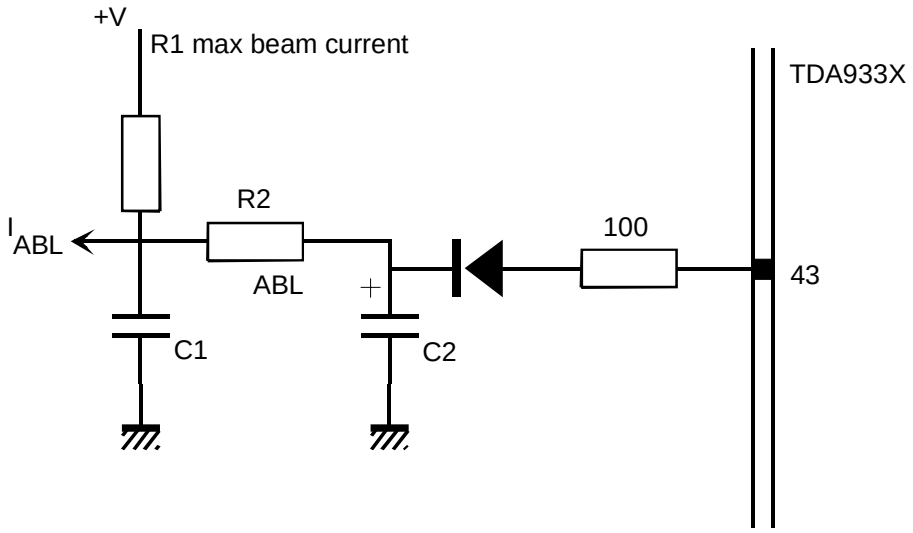


Fig 23 : Beam current limiting input - Standard application

*** RGB outputs pins 40, 41, 42**

The RGB outputs are supplied to the video output stages from pins 40, 41 and 42 respectively. For nominal input signals (i.e. CVBS/S-VHS, -(B-Y)/-(R-Y), TXT inputs) and for nominal control settings, then the RGB output signal amplitudes is typically $2V_{BLACK-WHITE}$. The maximum video output signals at these pins is Vcc-2V.

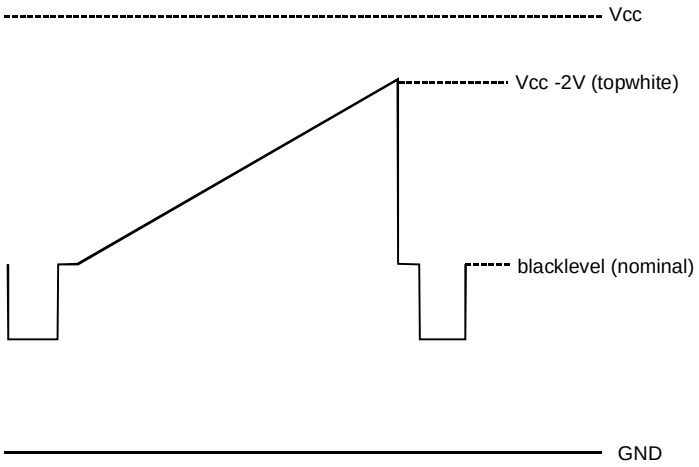


Fig 24 : Maximum RGB output

The DC level of the complete RGB signals, at RGB outputs, can be varied by varying VG2. The DC gain of the video output amplifiers should be chosen so that the DC level at RGB outputs during the black current measurement is approximately 2.5V when the VG2 DC control setting and cathode DC voltage are in their nominal operating region. Over the complete range of VG2 the cathode voltage should be above the cut-off of the CRT in order to avoid extra leakage during leakage measurement.

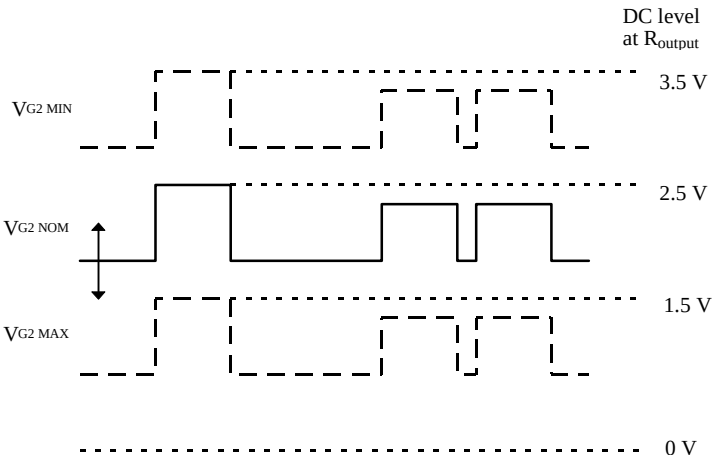


Fig 25 : Range RGB measuring pulses.

It is advised to minimise the capacitive loading of the RGB output pins, (i.e. series resistance's/inductance with RGB outputs).
For 1fh applications 100Ω series resistors are placed at the RGB output pins.

Besides these series resistor emitter followers are recommended at the RGB-outputs for 2fh application this to meet the bandwidth specification.

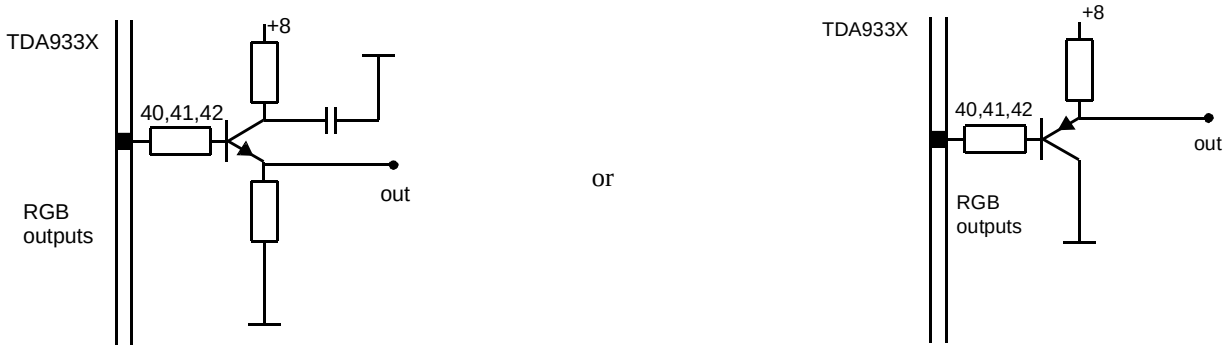


Fig 26 : Emitter follower to improve bandwidth

Side effects, for example temperature drift, of the these emitterfollowers will be handled (cancelled) by the black current loop (CCC-loop). If emitterfollowers are used the reference voltage at RGB-amplifiers should be compensated for the Vbe voltage drop of the emitterfollower. Also the DC-gain of the RGB-amplifier has to be adapted such that cut-off voltage in this new situation is equal to the situation without emitterfollower. This compensation is especially needed when the I^2C VG2 alignment bits **WBC** and **HBC** is used during factory alignment.

*** Black current input** **pin 44**

For correct operation of the CCC-loop Current information is supplied to the black current input pin

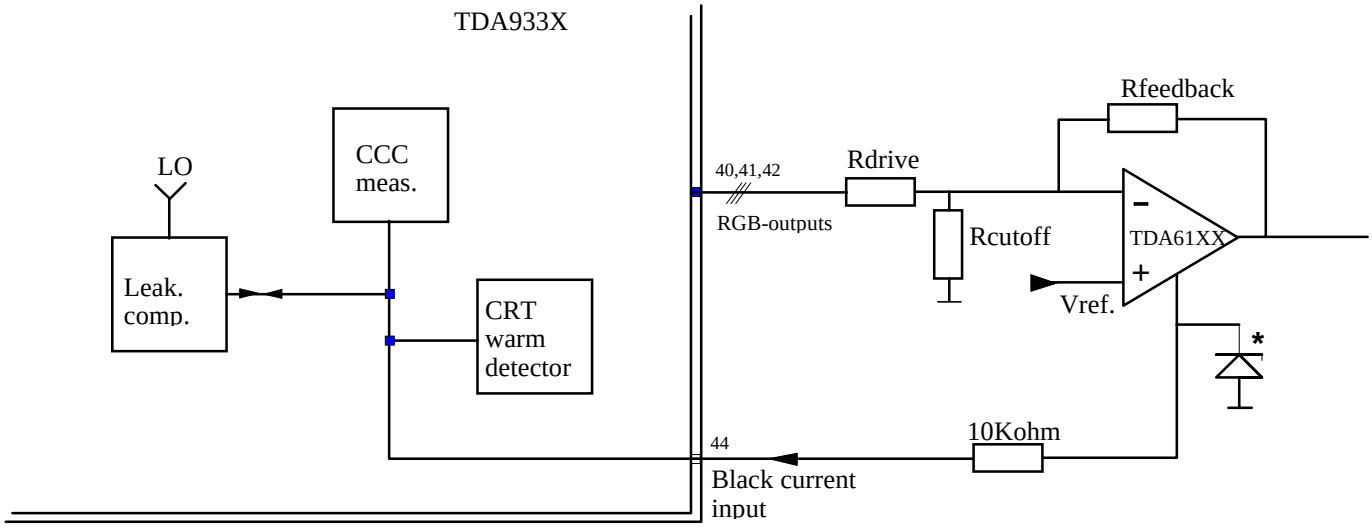


Fig 27 : Connecting RGB stage

* If a RGB output amplifier other then TDA6106/7/8 is used an external zener diode should be connected.

If the TDA6106/7/8 is used as RGB output amplifier an internal clamping diode, at 7V, prevents conduction of the internal protection diode of the TDA933X and thus prevents pollution of the internal 8V supply of the TDA933X.
For other types of RGB output amplifiers excessive video currents during scan has to be limited to maximum 300µA by connecting an external zener diode in the feedback path of the black current loop.

Hints for optimum CCC-loop performance:
- RGB-signal ground and large signal ground at the CRT-panel should be separated.
- Keep the gain of the RGB-amplifier as low as possible (Maximum RGB-signal output is Vcc-2V-DC level, ensure maximum RGB signal for maximum drive level at the cathode). A too high gain of the RGB amplifiers will be compensated by the CCC loop and can cause unstable loop behaviour.
- A small capacitor on the feedback line directly on the connector of the main board will suppress interference signals. For 2 Fh application the maximum allowed capacitor is 680pF. For 1 Fh application this value can be doubled.

If there is some signal bouncing present at the cathode of the picture tube then by means of a current divider further stability can be achieved. See figure below for this application.

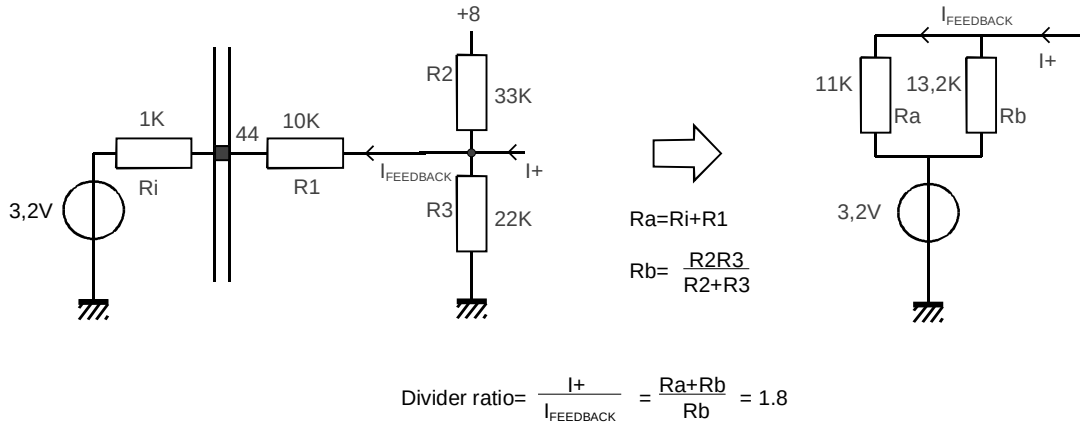
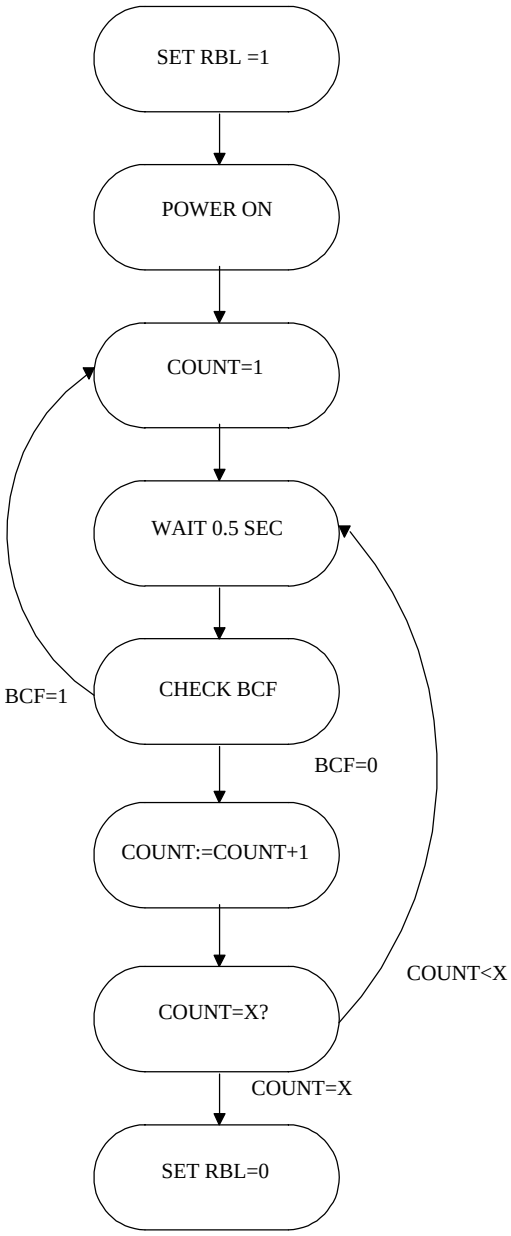


Fig 28 : Current divider in CCC loop

The voltage divider R2 / R3 should be designed for a voltage of 3.2 volt (equal to the internal reference voltage source) at the tiepoint. The voltage drop over Ri and R1 should be zero. Only then the above formulas are valid.
Due to this application the visibility of the measuring lines on the picture tube increase due to the fact that the total gain increases with the same ratio as the current divider divides the feedback current. Normally these measuring lines are in the overscan and therefore this is no issue. In the example the measuring currents at the cathode will increase from 8 µA and 20 µA to 14.4 µA and 36 µA (1.8 times higher)
For the same reason the RGB-signals at the cathodes will be amplified with the ratio of the current divider. But this effect can be compensated by lowering the **CL3..0** settings or with the **WPA R, G, B** registers.

It is also possible to use a resistive divider when a higher peak drive is needed than 95 Volt. The peak drive will be increased with the ratio of the current divider. In our example the 95 Volt drive becomes 171 Volt drive (1.8 times higher).

Start up behaviour.
The CCC-loop is optimised for fast release time of the RGB-outputs, therefore some discoloration or white smearing can occur on the picture screen during the release.
By means of the flowchart below the RGB-release can be delayed so the CCC-loop has more time to stabilise, what results in a improved RGB-release.



*** Fixed beam current switch -off (FBCSO) input pin 29**

This function is should only be used for picture tube without bleeder.
Besides the fact that the **FBC**-bit has to be set also a supply sense circuit has to be made in order to trigger the "fixed beam current switch-off " function . For this triggering it is best to monitor when the scan supply voltage for the horizontal deflection stage starts to decrease. The output signal of the scan supply sense circuit has to be applied to pin 29 of the TDA933X . Under normal operation the output signal has to be below the 1V ; whenever the voltage at pin 29 rises above the 2V the Fixed beam current function will be activated.
An example of a scan supply sense circuit is given in figure below.

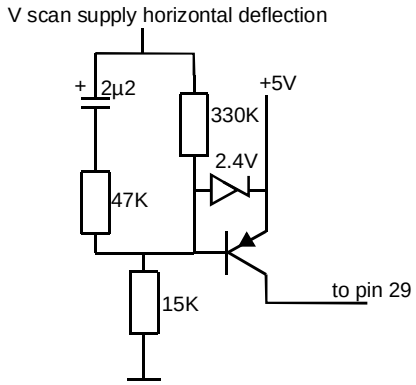


Fig 29 : Scan supply sense circuit

This circuit detects when the scan supply voltage starts to decrease and generates a signal for FBCSO-function.
It is important that the +5V has to remain stable as long as there is no **POR** generated or longer ; as long as there is **no POR** generated the fixed beam current switch-off will remain active.
When the pin is not used, it should be connected to ground.

Over the series resistor (10KΩ) at the black current input (pin44) a diode should be placed in order to make the discharge current of 1mA possible via the black current input.
Without this diode the voltage drop over the series resistor is too high (voltage drop: 1mA X 10KΩ =10V) so the fixed beam current switch-off function will not perform.

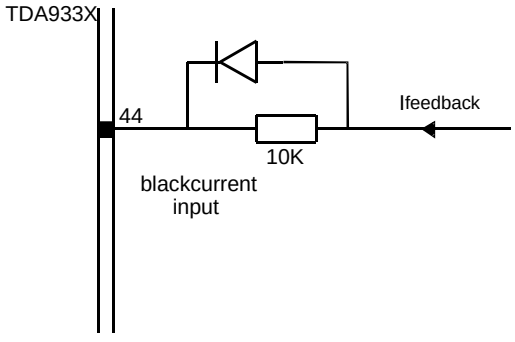


Fig 30 : Pin 43 application for FBSCO

3.2.4 Supply, decoupling and grounding

*** Grounding** **pin 6, 19**

For optimal performance we recommend to have both ground pins directly connected via a ground plane underneath the IC.

*** Digital supply decoupling** **pin 7**

This decoupling pin is for the supply of the digital circuits. The recommended capacitor value is 100 nF. Short decoupling to ground pin 6 is important to minimise interference.
The normal voltage on this pin is 5 Volt. When the voltage on pin 7 drops below 4,3 Volt, a **POR** is generated.

*** Supply,** **pin 17, 39**

The TDA933X has two supply pins 17 and 39. Both pins must be supplied simultaneously.
Notice that the IC has not been designed to use one of both pins as start pin. When switching on the power supply, the rise time at both pins should be equal. Therefore the time constants of the power supply decoupling should be the same.

The nominal supply voltage is 8V. With min/max. values of 7.2- 8.8V. The current consumption is about 22 mA for pin 17 and 28 mAfor pin 39.
In stand-by condition the 8V IC-supply can be switched off as to save energy. After switching on the 8V again the normal start-up procedure must be followed.

A voltage detection circuit is connected to both pins.
Power-up: if the 8V increases > 6.2 V than; (after IC-initialisation and auto re-calibration)
Hout starts via the slow start procedure
Hout continues at 1 Fh or 2 Fh, pending on the selected mode of operation

Power down: if the 8V drops < 6.2 V than; a power on reset, **POR**, is generated
The Hout is disabled immediate and
RGB outputs are blanked
IC must be re-initialised for correct re-start of the set

Short supply decoupling is important for a stable horizontal drive.

*** Bandgap decoupling,** **pin 18**

The bandgap circuit provides a very stable and temperature independent reference voltage and is used in almost all functional circuit blocks.
The reference voltage is 4,7 V. Optimal decoupling is achieved with two capacitors in parallel:
- Low frequent decoupling (for stable H-drive): C = 2.2 µF
- High frequent decoupling: C = 22 nF.

Short decoupling to pin 19 of the external capacitors is important.
During start-up the bandgap capacitor is pre-charged with 1mA during the first two vertical fields. If C=2.2µF, than t= 6.7V*2.2µ/1mA= 15ms.
A power on reset, **POR**, is generated when the voltage on pin 18 drops below 4,2V.

*** Pin protection for ESD** **all other pins**

Most IC-pins have internal protection diodes, one to supply and one to ground for ESD protection, see Fig 26 (see for exact configuration of specific pins the pin diagrams).
Under normal operation and supply-off condition these diodes may not conduct. Otherwise excessive current can flow through these diodes and/or internal circuit parts and the IC will be damaged.

All ESD protection diodes meet the specification of both Human body and Machine model.
Nevertheless for safe operation each pin voltage should remain in between:

- normal IC operation and supply is 8V: -0.5V …… +8.5V
- in stand-by condition and supply is 0V: -0.5V …… +0.5V

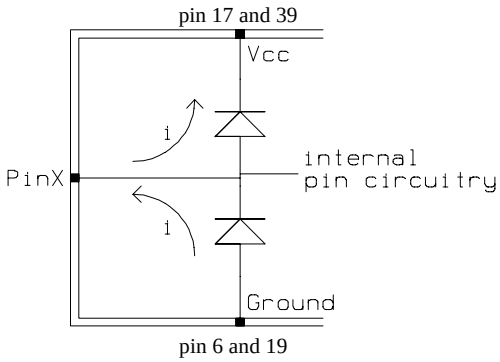


Fig 26: ESD pin protection

Note:
- When the supply =0V avoid that IC pins are supplied by e.g. the micro processor for OSD signals.
  We have had no problems so far when the a continuous diode current is less than 1mA.
- Maximum voltage for Y/U/V pins (28, 27, 26) is 5.5V. This to avoid parasitic effect at the pin.

3.3 Application of non-used pins

Below the preferred application is given for pins, which are not used.

Pin	Name	Application
3	E/W drive	Connect to +8 Volt supply
4	EHT compensation/Overvoltage	Apply resistive divider at 2 Volt + capacitor 100 nF to ground
5	Flash	Connect to ground
14	Dynamic phase compensation	Apply 100 nF capacitor to ground
22	Low power start-up	Connect to ground
25	DAC out	Leave open
29	Fixed beam current switch-off	Connect to ground
33	Fast blanking RGB1	Apply 560 Ohm to ground
34	Peak white limiting	Apply 10 pF to ground
38	Fast blanking RGB2	Apply 560 Ohm to ground
43	BCL	Apply resistive divider at 3.3 Volt
44	Black current input (**AKB** = 1)	Leave open

4. ALIGNMENTS

4.1 Colour temperature alignment

The colour temperature is aligned via the I^2C registers **WPA (R,G,B)**
For a correct alignment take notice of the following:
-Use a high quality videogenerator (a service generator is not preferred)
-Don't use a full white field, but a signal with a white block (of 20%).
-Be sure that the picture tube is adequate degaussed.
-All features should be switched off (especially the blue stretcher)
-Vg2 should be correct aligned.
-Align the White point registers at **low light,** for example around 10cd/m^2, this to avoid side effects at a certain **high light** (for example saturation of the phosphor). Adapt the lighting condition to prevent influence of ambient light
-Put the saturation control to 00
-Blue register of the WPA is kept constant the Red register correspond with the x-coordinate of the CIE 1931 plane, the green register correspond with the y-coordinate of the CIE 1931 plane.

4.2 Geometry alignment

Alignment of horizontal and vertical geometry

For optimal geometry, it is important to align the vertical and horizontal registers in the correct sequence.
It is very important to align always **VS** (vertical slope) and **VSH** (vertical shift) as indicated below to ensure correct performance under all circumstances. Because these registers are meant to compensate for the tolerances of the total deflection system, the spreads as found in practice do not allow to load these registers with a fixed value without aligning.

- Load registers for zoom and scroll with the correct value:
  Set **VX** (vertical expand, reg. 17 hex, bit D5..0) : 19 hex
  Set **VSC** (vertical scroll, reg. 18 hex, bit D5..0) : 1F hex
  If not set correct, the specified zoom/scroll ranges are not valid. Also problems can occur with too early blanking at the top or bottom of the screen.

- Set **SC** (S-correction, reg. 15 hex, bit D5..0) with predetermined value
  The value of the vertical S-correction is related to the screen curvature and once determined this will not change for the same model picture tube. For each different tube model, a specific S-correction value has to be determined.
  The needed value of this register can range between 0 and 63, pending on the screen curvature. There is no problem when the determined value is close to the end of the adjustment range, because there is no spread.

- Apply a video pattern with a horizontal line in the middle (e.g. a suitable X-hatch)

- Switch-on the service blanking:
  Set **SBL** (service blanking, reg. 00 hex, bit D5) = 1
  The service blanking blanks the bottom half of the picture. The blanking starts at the point where the differential current of the vertical drive outputs becomes zero, so at the point where the vertical deflection is zero.

- Adjust the vertical slope:
  Align **VS** (vertical slope, reg. 13 hex, bit D5..0) till the horizontal line in the centre of the video signal is just at the position where the blanking starts.
  This alignment is very important, because it calibrates the peak-to peak value of the generated sawtooth at pin 15. The correct peak to peak value is important, because several other correction signals are derived from this sawtooth.
  This alignment compensates for the following spreads:

- Spread on the component value of the sawtooth capacitor at pin 15 (major)
- Spread on the sawtooth current (minor)

- Switch-off the service blanking
  Set **SBL** (service blanking, reg. 00 hex, bit D5) = 0

- Adjust the vertical shift:
  Align **VSH** (vertical shift, reg. 16 hex, bit D5..0) till the picture is centred. If the picture tube has a marking in the middle, it is also possible to align the horizontal line in the middle with the markings.
  This alignment is important to obtain the correct waveforms for the East-west correction signals and the right S-correction.
  This alignment compensates for the following spreads:
  - DC-offset of the vertical deflection amplifier (major)
  - Vertical mechanical offset of the picture tube gun (minor)
  - DC offset of the vertical drive outputs (minor)

After these alignments the system has been made “tolerance free” which ensures the correct performance.

- Adjust the vertical amplitude:
  Align **VA** (vertical amplitude, reg. 14 hex, bit D5..0) till the picture height is correct.

The three alignments above influence the horizontal East-West waveforms, so it is important to carry out these vertical alignments first before starting the horizontal (East-West) alignments.

- Adjust the horizontal shift
  Align **HSH** (horizontal shift, reg. 0C hex, bit D5..0) to centre the picture horizontal

- Adjust the horizontal width
  Align **EW** (East-West width, reg. 0E hex, bit D5..0) to adjust the correct width (use the width of the horizontal line in the centre to determine the final picture width)

- Adjust the size of the East-West parabola
  Align **PW** (parabola width, reg. 0F hex, bit D5..0) to straighten the vertical lines at the sides.

- Correct (if necessary) trapezium distortion
  Align **TC** (trapezium correction, reg. 11 hex, bit D5..0) to set the lines at the sides vertical

- Correct (if necessary) corner distortion
  Align **CP** (corner parabola, reg. 10 hex, bit D5..0) to straighten the top and bottom of the vertical lines at the sides.

- Correct (if necessary) parallelogram distortion
  Align **HP** (horizontal parallelogram, reg. 0D hex, bit D5..0) to set vertical lines orthogonal to the horizontal lines.

The order of aligning the horizontal parameters is not so critical, once the vertical alignment is done correctly.

It is of course always possible before starting alignment to preload all geometry registers with values, close to the expected value, to save time during the alignment.

5. REMARKS FOR THE TDA 933X N1 VERSION

1. Switching to VGA mode and back
2. Blue stretch function
3. N2 version

1. Switching to VGA mode and back (Only valid for TDA 9331/2)

Due to a problem in the vertical divider, it is possible that the vertical outputs stop when switching from TV mode to VGA mode or from VGA mode back to TV mode. When this happens, the TDA933X does not respond to I^2C commands any more.

This problem only occurs when both conditions below are met:
- The I^2C message to switch over from TV mode to VGA mode (settting **VGA** = 1) or to switch-over from VGA mode to TV mode (setting **VGA** = 0) is given during the vertical retrace
- There is no valid H_D and/or V_D pulse present

The problem can be avoided when care is taken to switch only to VGA mode or TV mode (toggling the **VGA**-bit) when valid H_D **and** V_D pulses are present.
The requirements for valid H_D and V_D pulses are:
- For valid H_D pulses, at least one pulse every three lines.
  This is for 1 Fh, at least one H_D pulse every 192 µs.
  This is for 2 Fh, at least one H_D pulse every 96 µs.
- For valid V_D pulses, at least one pulse every three fields.
  This is for 1 Fv at least one V_D pulse every 16.6 ms.
  This is for 2 Fv at least one V_D pulse every 8.3 ms.

The requirements are such, that H_D and V_D pulses from a scan converter or an input processor, even under free running or noisy conditions will fulfil the above requirements.

To prevent problems, the software routines should be adapted for the following conditions:
- Switch-on from stand-by setting **STB1,0** to 1 1
- Switching off to stand-by setting **STB1,0** to 0 0 (while the + 8 Volt remains present)
- Switching from TV-mode to VGA mode setting **VGA** = 1
- Switching from VGA mode to TV mode setting **VGA** = 0

Switch-on from stand-by setting **STB1,0** to 1 1
Because the TDA9331,2 always starts-up in TV mode when switched on from stand-by, VGA should be set to 0 when switching on from stand-by by setting **STB1,0** to 1 1. If **VGA** is set to 1 before switching on from stand-by, the TDA9331,2 will switch over automatically to VGA mode once the PHI-2 is locked. To prevent that this happens before valid H_D and V_D pulses are present, **VGA** should be set to 0.

Routine
- Check till **POR** = 0 and **NRF** = 0
- Write all I^2C registers with **STB1,0** = 1 1 and **VGA** = 0

Do not set **VGA** = 1 until valid H_D and V_D pulses are present

Switching off to stand-by setting **STB1,0** to 0 0 while in **VGA** mode (while the + 8 Volt remains present)
When switching to stand-by, the TDA9331,2 switches back to TV mode before starting the slow stop procedure. Therefore **VGA** must be set to 0 before switching to stand-by setting **STB1,0** to 0 0.

Routine
- Ensure that valid H_D and V_D pulses are present
- Set **VGA** = 0
- Wait 2 fields
- Set **STB1,0** = 0 0

Switching from TV-mode to VGA mode setting **VGA** = 1
The VGA input is usually a seperate input. To prevent problems when no signal is connected to the VGA input (no H_D and V_D pulses present), switch over to VGA mode while still connected to the H_D and V_D pulses of the input processor or scan converter.

Routine
- Ensure that valid H_D and V_D pulses are present from the scan converter of the input processor
- Set **VGA** = 1
- Wait 2 fields
- Switch the H_D and V_D inputs to the VGA input

Switching from VGA mode to TV mode setting **VGA** = 0
For the same reason as above (it is possible that no device is connected to the VGA input, so no H_D and V_D pulses are present) switch first back to the H_D and V_D pulses of the input processor or scan converter before switching back to TV mode.

Routine
- Switch the H_D and V_D inputs back to the scan converter of the input processor
- Wait 2 fields
- Set **VGA** = 0

2. Blue stretch function

The blue stretch function does not work in the TDA933X N1. Due to a design mistake, the threshold level for activating the blue stretch is set too high. In practice, activating the blue stretch function does not give a visable effect.

3. N2 version

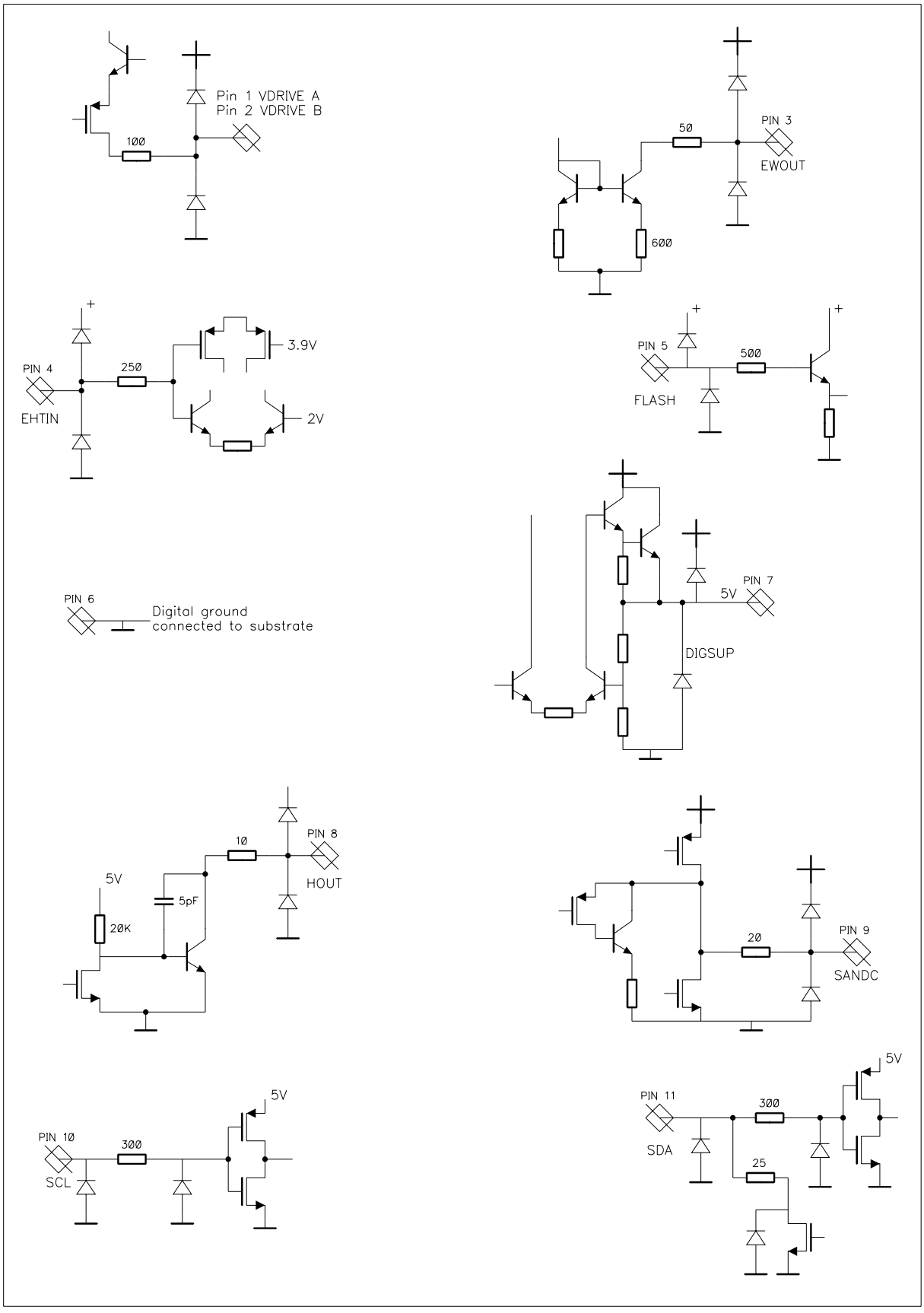
Both above mentioned problems will be corrected in the N2 version of the TDA933X.

6. REFERENCES

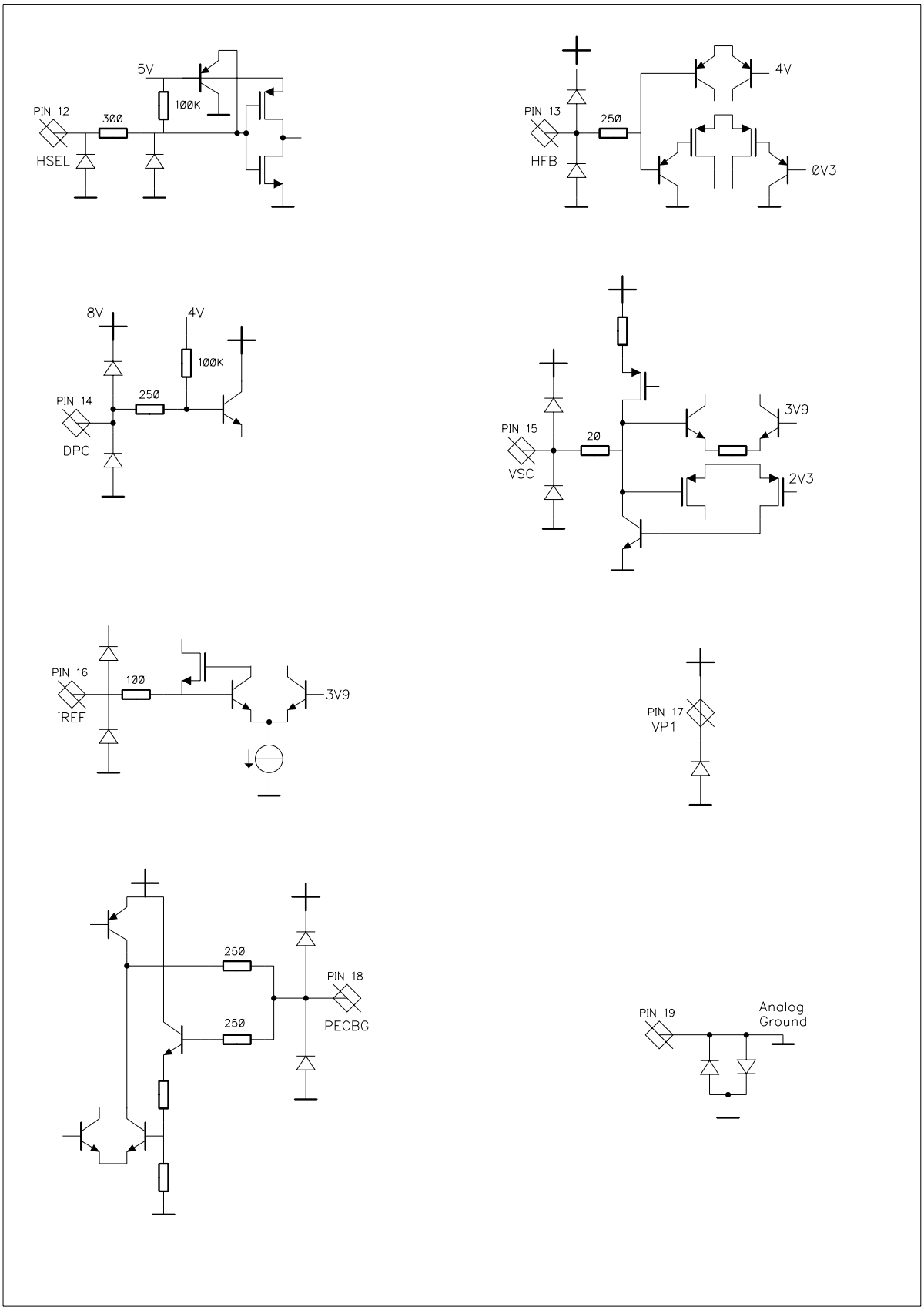
1. Device Specification, June 2, 1998.
TDA933XH I²C-bus controlled TV Display Processors.

2. Device Specification, may, 1998.
TDA9320H I²C-bus controlled TV input Processor.

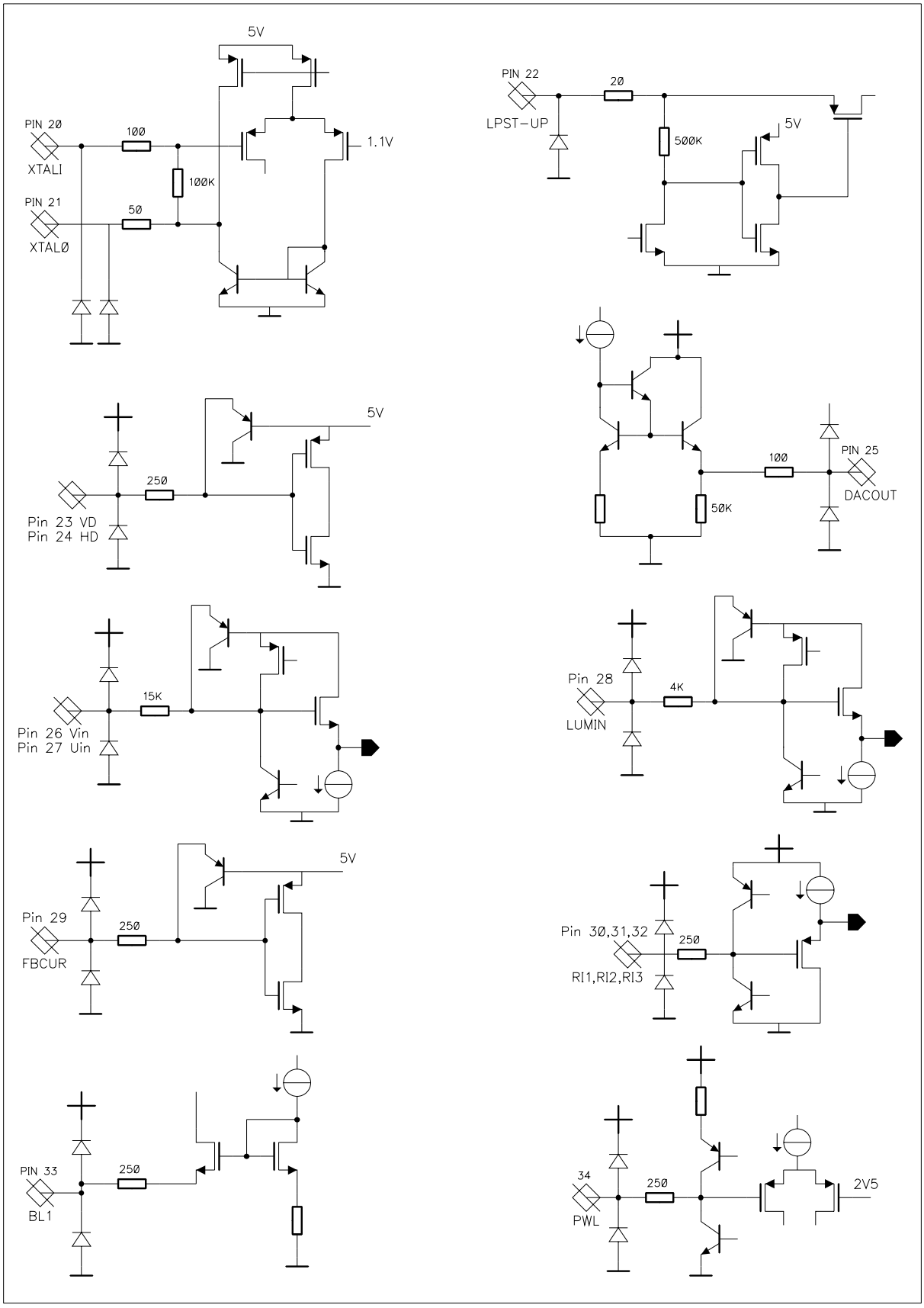
3. TDA8350 and TDA8351 deflection output circuits application information.
Report no AN95029.



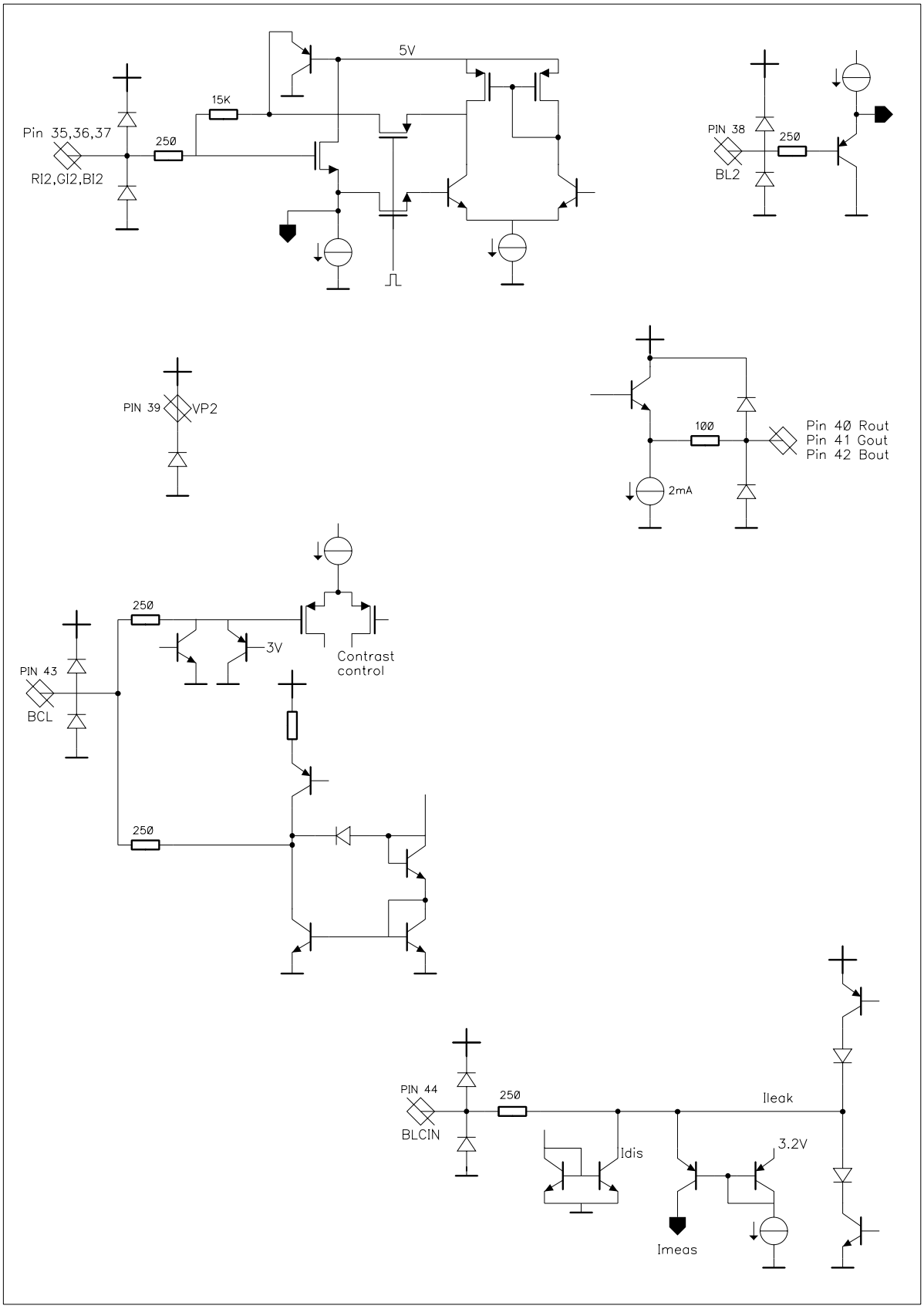
B 1 : Internal pinning diagram (1-11)



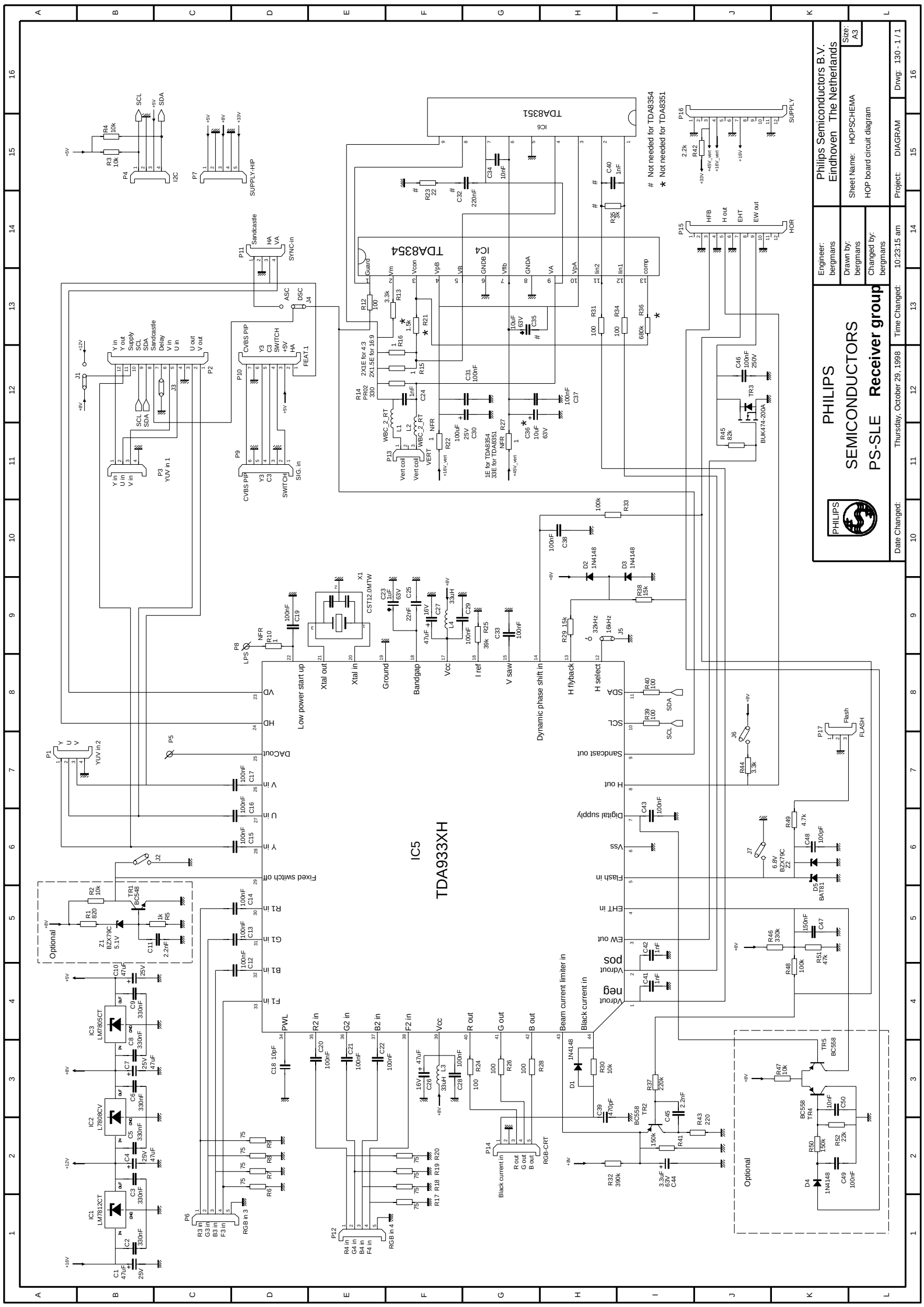
B 2 : Internal pinning diagram (12-19)



B 3 : Internal pinning diagram (20-34)



B 4 : Internal pinning diagram (35-44)



C 1 : Application diagram of TDA933X